DECEMBER 1986 VOL. 4, NO. 12 $3.95

FOR IBM PERSONAL COMPUTER USERS

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Technology, Hardware, Software

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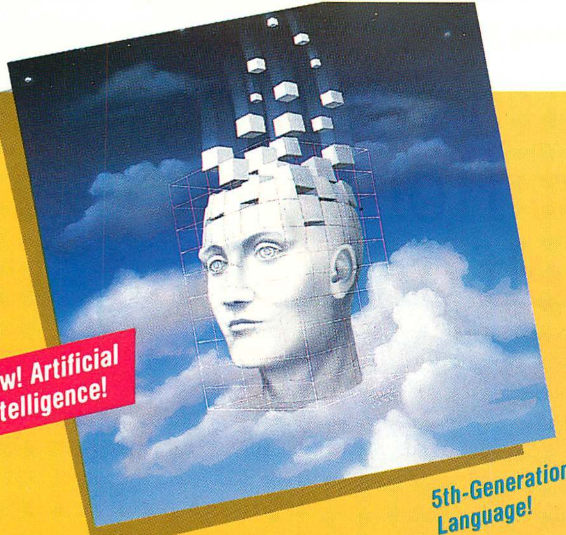
BASIC COMPILERS



New! Artificial Intelligence!

5th-Generation Language!

$10.00 Scratch 'n Win Rebate!

Turbo Prolog™

"If you're at all interested in artificial intelligence, databases, expert systems, or new ways of thinking about programming, by all means plunk down your $100 and buy a copy of Turbo Prolog."
Bruce Webster, BYTE

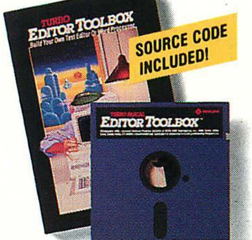
"Borland International, Inc. is gunning onto the fast track in the artificial intelligence and engineering-language-software race, riding aboard a new $99 Turbo Prolog," says Tom Schwartz in *Electronic Engineering Times.* And so we are. Our new Turbo Prolog has drawn rave reviews—which we think are well deserved—because Turbo Prolog brings 5th-generation language and supercomputer power to your IBM PC and compatibles. Turbo Prolog is a high-speed compiler for the artificial intelligence language, Prolog, which is probably one of the most powerful programming languages ever conceived. We made a worldwide impact with Turbo Pascal and you can expect the same results and revolution from Turbo Prolog, the natural language of artificial intelligence. Darryl Rubin, writing in *AI Expert* said, *"Turbo Prolog offers generally the fastest and most approachable implementation of Prolog."* Suggested retail, $99.95. Use a $10.00 Scratch 'n Win Rebate and that goes down to only *$89.95!* Minimum memory: 384K.

Technical Specifications:

TURBO PASCAL 3.0 Minimum memory: 128K; includes 8087 and BCD features for 16-bit MS-DOS and CP/M-86 systems. CP/M-80 version minimum memory: 48K; 8087 and BCD features not available. ***TURBO DATABASE TOOLBOX*** Minimum memory: 128K. CP/M-80 minimum memory: 48K. Requires Turbo Pascal 2.0 or later. ***TURBO GRAPHIX TOOLBOX**** Minimum memory: 192K. Requires PC/MS-DOS 2.0 or later, Turbo Pascal 3.0, and IBM CGA, Hercules Monochrome Card or equivalent. ***TURBO TUTOR 2.0*** Minimum memory: 192K. CP/M-80 version minimum memory 48K. Requires PC/MS-DOS 2.0 or later and Turbo Pascal 3.0. ***TURBO EDITOR TOOLBOX**** Minimum memory: 192K. Requires PC/MS-DOS 2.0 or later and Turbo Pascal 3.0. ***TURBO GAMEWORKS**** Minimum memory: 192K. Requires PC/MS-DOS 2.0 or later and Turbo Pascal 3.0. ***TURBO PROLOG**** Minimum memory: 384K. ***REFLEX: THE ANALYST**** Minimum memory: 384K. Requires IBM CGA, Hercules Monochrome Card or equivalent. Works with Intel's AboveBoard-PC and -AT; AST's RAMpage! and RAMpage! AT; Quadram's Liberty-PC and -AT; Tecmar's 640 Plus; IBM's EGA and 3270/PC; AT&T's 6300 and many others. ***REFLEX WORKSHOP**** Minimum memory: 384K. Requires Reflex: The Analyst. ***TURBO LIGHTNING**** Minimum memory: 256K. Two disk drives required. Hard disk recommended. ***LIGHTNING WORD WIZARD**** Minimum memory: 256K. Requires Turbo Lightning. Turbo Pascal 3.0 required to edit source code. ***SIDEKICK**** Minimum memory: 128K. ***TRAVELING SIDEKICK**** Minimum memory: 256K. ***SUPERKEY**** Minimum memory: 128K. *For IBM PC, AT, XT, PCjr and true compatibles only, running PC/MS-DOS 2.0 or later.

Turbo Pascal Programming

Build Your Own Word Processor!



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Turbo Editor Toolbox™

Recently released, we called our new Turbo Editor Toolbox a "construction set to write your own word processor." Peter Feldmann of *PC Magazine* covered it pretty well with, *"A 'write your own word processor' program for intermediate level programmers, with lots of help in the form of prewritten procedures covering everything from word wrap to pull-down windows."* Source code is included, and we also include MicroStar, a full-blown text editor with pull-down menus and windowing. It interfaces directly with Turbo Lightning to let you spell-check your MicroStar files. Jerry Pournelle of *BYTE* magazine said, *"The new Turbo Editor Toolbox is the Turbo Pascal source code to just about anything you ever wanted a PC-compatible text editor to do."* Suggested retail: $69.95. Use a $10.00 Scratch 'n Win Rebate and you'll get all this for *only $59.95!* Minimum memory: 192K.

MicroStar file directory accessed by pull-down menu

Borland's Business Productivity Programs:

Reflex: The Analyst® Analytical database manager. Provides complete, new look at data normally hidden by programs like 1-2-3® and dBASE.® Best report generator for, and complement to, 1-2-3.

Reflex Workshop™ Important new addition to Reflex: The Analyst. Gives you 22 different templates to run your business right.

SideKick® Complete RAM-resident desktop management includes notepad, dialer, calculator and more.

Traveling SideKick® Electronic version of business/personal diaries, daytime organizers; works with your SideKick files; important professional tool.

SuperKey® Keyboard enhancer. Simple macros turn 1000 keystrokes into 1. Also encrypts your files to keep confidential files confidential.

Borland's Electronic Reference Programs:

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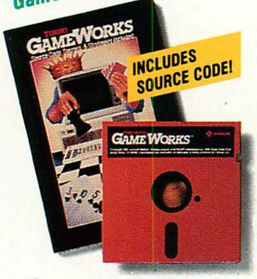
Lightning Word Wizard™ Includes ingenious crossword solver and six other word challenges. If you're into programming, Lightning Word Wizard is also a development toolbox and the technical reference manual for Turbo Lightning.

Turbo Pascal Programming

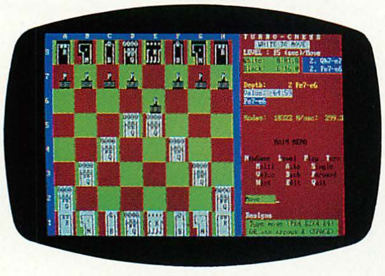
Learn Secrets, Strategies, Game Theory!



$10.00 Scratch 'n Win Rebate!

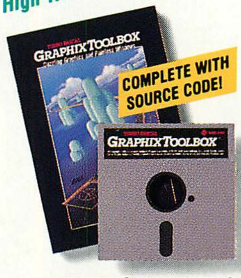
Turbo GameWorks®

Also recently released, Turbo GameWorks is what you think it is: "Games" and "Works." Games you can play right away (like Chess, Bridge and Go-Moku), plus the Works—which is how computer games work. All the secrets and strategies of game theory are there for you to learn. You can play the games "as is" or modify them any which way you want. Source code is included to let you do that, and whether you want to write your own games or simply play the off-the-shelf games, Turbo GameWorks will give hours of diversion, education, and intrigue. George Koltanowski, Dean of American Chess, and former President, United States Chess Federation, reacted to Turbo Game-Works like this: "*With Turbo GameWorks, you're on your way to becoming a master chess player.*" And Kit Woolsey, writer, author, and twice Champion of the Blue Ribbon Pairs, wrote, "*Now play the world's most popular card game—Bridge . . . even program your own bidding and scoring conventions.*" Suggested retail: $69.95. Use a $10.00 Scratch 'n Win Rebate and you're talking an *incredible $59.95!* Minimum memory: 192K.



Turbo GameWorks' Chessboard

Create Your Own High-Res Graphics!



$10.00 Scratch 'n Win Rebate!

Turbo Graphix Toolbox®

It includes a library of graphics routines for Turbo Pascal programs. Lets even beginning programmers create high-resolution graphics with an IBM, Hercules,™ or compatible graphics adapter. Our Turbo Graphix Toolbox includes all the tools you'll ever need for complex business graphics, easy windowing, and storing screen images to memory. It comes complete with source code, ready to compile. Suggested retail: $69.95, but with a $10.00 Scratch 'n Win Rebate, *only $59.95!* Minimum memory: 192K.

The Ultimate Learning Experience!

$10.00 Scratch 'n Win Rebate!

Turbo Tutor® 2.0

COMPLETELY NEW VERSION!

The new Turbo Tutor can take you from "What's a computer?" through complex data structures, assembly languages, trees, tips on writing long programs in Turbo Pascal, and a high level of expertise. Source code for every-thing is included. New split screens allow you to put source text in the bottom half of the screen and run the examples in the top half. There are quizzes that ask you, show you, tell you, teach you. You get a 400-page manual—which is not as daunting as it sounds, because unlike many software manuals, it was not written by orangutans. Suggested retail: $39.95. Use a $10.00 Scratch 'n Win Rebate and you're down to an *unheard of $29.95!* Minimum memory: 192K.

Recognition for Borland International has come from business, trade, and media, and includes both product awards and awards for technical excellence and marketing.

America's Cup. Coming Soon!

How to use Scratch 'n Win Rebates

It's really simple. You purchase the product between 9/5/86 and 3/31/87, and return the license agreement along with dated proof of purchase and your rebate card. We'll mail you a check for $10.00 on single product purchases or a check for $15.00 when you buy an advertised "bundle"—which means our Turbo Pascal Jumbo Pack, or Turbo Lightning and Lightning Word Wizard, or Reflex: The Analyst and Reflex Workshop, or SideKick and Traveling SideKick. (Restrictions do apply. See Official Rules on back of Instant Winner card).

Sail designs generated from Shore Sails' Turbo Pascal programs.

Borland's award-winning software is the best Holiday present you can give yourself or anyone else

Any one of these Holiday presents could save your marriage, career, reputation and quite a few bucks.

When you give or get any one of these Holiday presents, every day's a Holiday, because you're giving or getting long-lasting software that's a lot more welcome to the Woman in your Life than vacuum cleaners, egg-beaters and ugly earrings. And the Man in your Life would rather have Turbo Prolog,™ Reflex,® Reflex Workshop,™ Turbo Pascal,® Turbo Lightning® or SideKick® than socks, ties and wrong-size shirts.

Turbo Prolog takes you by the hand into the brave new world of Artificial Intelligence

Artificial Intelligence is no substitute for the human brain (well, most human brains; you make your own list), but it is a fascinating new field, and we're leading it with our 5th-Generation Turbo Prolog. In fact, people are telling us that Turbo Prolog is "The most exciting product they've seen this year." So see it for yourself. Give it. Get it. You deserve it.

Turbo Pascal wins PC World's 1986 World Class PC Award for 'Programming Language'!

Give someone our Turbo Pascal "Jumbo Pack," but keep some of the precious pieces for yourself

There's so much in there—Turbo Pascal, Turbo Tutor,® Turbo Database,™ Turbo Graphix,® Turbo GameWorks,® Turbo Editor®—you can probably give someone else one or two of them. (Just keep the ones you don't have already and make the rest thoughtful, really inexpensive presents for someone's Turbo Pascal library.)

Give them one, maybe two kinds of Holiday Reflex action!

Adam B. Green, InfoWorld's highly respected columnist, says "*Everyone agrees Reflex is the best-looking database they've ever seen.*" Peter Norton of PC WEEK says, "*The next generation of software has officially arrived.*" And now, with our brand-new Reflex Workshop, which includes 22 instant ways to run your business well, you can give someone both programs and just about guarantee them a Happy well-run New Year!

Turbo Lightning wins the 1986 World Class PC Award for "Most Promising Newcomer"!

Solve your gift-giving and spelling problems now with Turbo Lightning

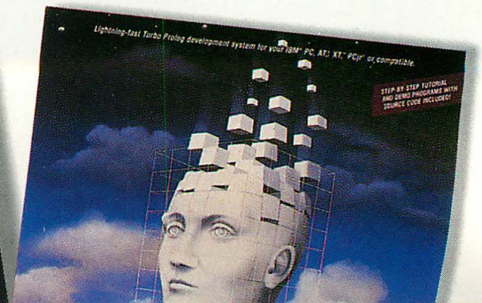
While you use SideKick, Reflex, Lotus 1-2-3® and most popular programs, Turbo Lightning proofreads *as you write*! If you misspell a word, Turbo Lightning will beep at you instantly, and suggest a correction for the word you just misspelled. Press one key, and the misspelled word is immediately replaced by the correct word. And if you're ever stuck for a word, Turbo Lightning's thesaurus is there with instant alternatives. Perfect gift for everyone who reads and writes!

Attention SideKick users! Your SideKick now has a sidekick!

If you're going anywhere for the Holidays, you'll need a Traveling SideKick!

It's the electronic organizer for this electronic age—a professional binder, a software program and a report generator—a modern business tool that prints your ever-changing appointments in daily/weekly/monthly/yearly form. Your appointments, phone list, address list, meeting schedule, travel itinerary—even your mailing list—can be kept up-to-the-minute correct *and with you*! (SideKick Owners: All your files translate instantly to Traveling SideKick.) Traveling SideKick is electronic, so it's good for this year, next year and all the next years after that—it's not a dusty old diary that dies Dec. 31!

BI-1075C



OFFICIAL RULES - BORLAND INSTANT WINNER GAME

1. NO PURCHASE NECESSARY: To participate, you may obtain a game card inserted into the October, November, December, or January issue of the following magazines: PC World; Byte; PC Tech Journal; PC Magazine. You may also obtain a game card by mailing a self-addressed, stamped envelope to: Borland International Game Card, P.O. Box 870, Wilton, CT 06897. (Washington State residents send self-addressed envelope.) Limit one game card per stamped request. All requests must be received by January 15, 1987.

2. TO PLAY: Remove the rub-off area on the game card to reveal what prize or rebate offer you have obtained.

3. PRIZES/ REBATES: Beneath the rub-off area one of the following prizes may be revealed: Trip for Two to America's Cup Races or $10,000; 1986 Suzuki 4W Samurai Convertible or $6,895; AST Turbo Laser, Toshiba 1100 Portable Computer, Toshiba 3100 Portable Computer, AST Sixpakpremium; AST Advantagepremium; AST 3G Pak; AST Rampage; AST Rampage AT; Free Borland Product, or you may obtain the following rebate offer: $10 rebate offer on any individual product or $15 rebate offer on any single advertised Borland bundle (See rule #11 for prize details.).

4. PRIZE CLAIMS: If you obtain one of the prizes stated in Rule #3, sign your full legal signature on the game card and send via certified mail (copy should be made for your records) along with your name and address to: Borland International Prize Claim, 196 Danbury Road, Wilton, CT 06897. All prize claims must be received or postmarked by February 15, 1987. (See Rule #12 for Trip for Two to America's Cup exception.)

5. REBATE CLAIMS: Rebates are good for products purchased from September 5, 1986 through March 31, 1987. The $10 rebate is good for any individual Borland product and the $15 rebate is good for any advertised Borland software bundle. To receive your rebate you must return your completed license agreement from the manual, this game card and dated proof of purchase to: Borland International, Game Card Rebate, 4585 Scotts Valley Drive, Scotts Valley, CA 95066. Upon receipt of the license agreement, game card and proof of purchase, Borland will send your check. Rebate is not valid with any other rebate or promotion offered directly from Borland.

6. VERIFICATION: All game materials are subject to verification. Game materials are void and will be rejected if not obtained through authorized, legitimate channels, and may be rejected if any part is reproduced, counterfeited, torn or altered in any way, or if materials contain printing, typographical, or mechanical errors. Decisions of the Redemption Center are final. Game pieces from any game other than the Borland Instant Winner Game may not be used in this game.

7. CONDITIONS OF PARTICIPATION: Material submitted becomes the property of Borland International. The submission of game pieces is the sole responsibility of the individual seeking verification, who is solely responsible for lost, late, or misdirected mail. All taxes, registration and inspection fees are the sole responsibility of the verified winner. Winners may be required to execute an affidavit of eligibility and name and likeness publicity release. By participating in the game you accept and agree to be bound by these rules and the decision of the Official Redemption Center which will be final.

8. ELIGIBILITY: Participation is open solely to residents of the United States 18 years of age and over, except employees and agents of Borland International, service agencies, and individuals engaged in the development, production, or distribution of game materials, The Merritt Group, Inc. and their immediate family or members of their households. Void in Vermont and where prohibited by law.

9. GAME SCHEDULE AND AWARD OF PRIZES: The Borland Instant Winner Game will commence on or about September 5, 1986 and end on January 30, 1987. It will officially end, however, when all game pieces are distributed. Verified game prizes will be awarded within thirty (30) days from the date of their receipt for verification at the Official Redemption Center. A major prize winners' list can be obtained by sending a stamped, self-addressed envelope to: Borland Instant Winner Game Winners' List, P.O. Box 7089, Wilton, CT 06897.

10. ODDS CHART: The odds of winning prizes are based upon obtaining the one rare game piece among the applicable number of game pieces.

PRIZE	Qty.	Total Value	Odds of Winning
Trip for Two to America's Cup or $10,000	1	$ 10,000.00	1 in 6,458,000
Suzuki 4W Samurai Convertible JA or $6,895	2	$ 13,790.00	1 in 3,229,000
AST Turbo Laser	1	$ 4,995.00	1 in 6,458,000
Toshiba Portable Computer	2	$ 6,898.00	1 in 3,229,000
AST Memory Boards	25	$ 15,025.00	1 in 258,320
Borland Products	1,000	$149,000.00	1 in 6,458
OVERALL TOTAL	1,031	$199,708.00	1 in 6,264

All remaining game cards will contain a $10 rebate good on any individual Borland product or a $15 rebate good toward any advertised Borland software bundle.

11. PRIZE DETAILS: Trip for two to America's Cup Races (or $10,000) will include coach seating round trip airfare on regularly scheduled commercial airline from San Francisco, California to Perth, Australia and up to two weeks hotel accommodations in Perth, Australia plus $4,500 spending cash. Winners will be responsible for obtaining visa, passport, and all other travel documents. Trip does not include meals, taxes, excess baggage charges and other hotel charges. Minor must be accompanied by parent or legal guardian.

Suzuki 4W Samurai Convertible JA Standard Equipment Package (or $6,895), verified winner will be responsible for all registration, insurance, and licensing fees. AST Turbo Laser, Toshiba Portable Computer Model #T1100; Toshiba Portable Computer Model #T3100; AST Memory Boards and Free Borland Products are non-substitutional except by sponsor due to product availability and all warranties and guarantees are subject to manufacturers terms. All prizes are non-transferrable. Winning consumer is responsible for all local, state and federal taxes.

12. SECOND CHANCE SWEEPSTAKES: There are two Second Chance Sweepstakes drawings scheduled to be conducted on December 31, 1986 and February 28, 1987. Random drawing from all entries received by December 30, 1986 will award trip for two to America's Cup Races (or $10,000). Random drawing from all entries received by February 26, 1987 will award two (2) Suzuki 4W Samurai (or $6,895). All remaining prizes that are unclaimed after February 15, 1987 will remain unclaimed. Send entry to: Second Chance Entry P.O. Box 870 Wilton, CT 06897.

If you have any questions concerning the Borland Instant Winner Game, call: 1-800-451-4471.

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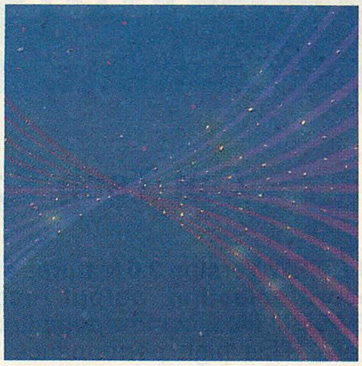

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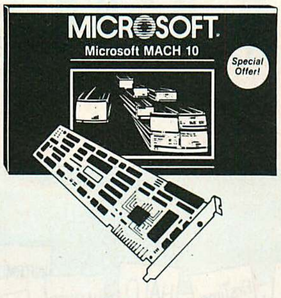

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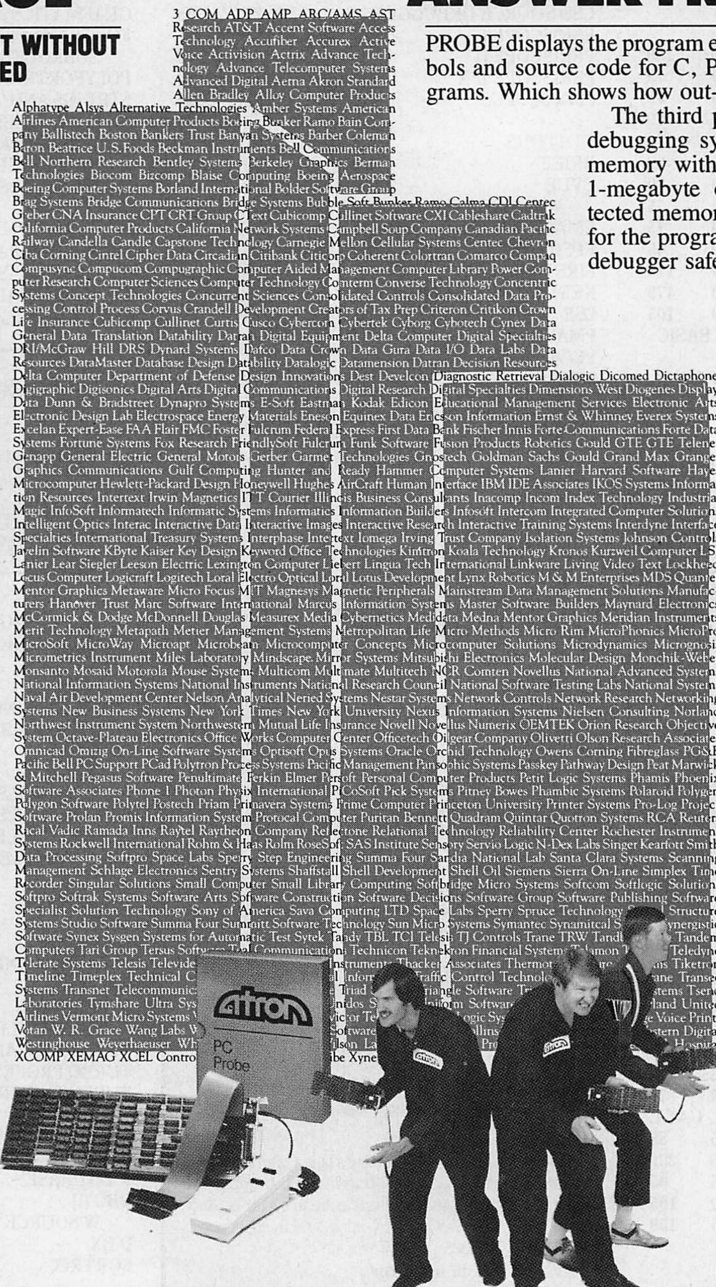

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PLAGUES OF BIBLICAL PROPORTIONS

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Second came the plague of not knowing where the program was, or where it had recently been. This compounded the first plague: How could anyone know *what* caused the random memory overwrites? Add to this random interrupts and timing dependencies, and you begin to understand *The Fear* that gripped the city.

Then came the last plague, which brought the wizards to their knees before they even started debugging. Their towering programs consumed so much memory, there wasn't enough room for their symbol table, let alone debugging software. Even if they could get past the first two plagues, this one killed their firstborn software.

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The RT Mystery

Is it IBM's next architecture, or just another incidental machine?

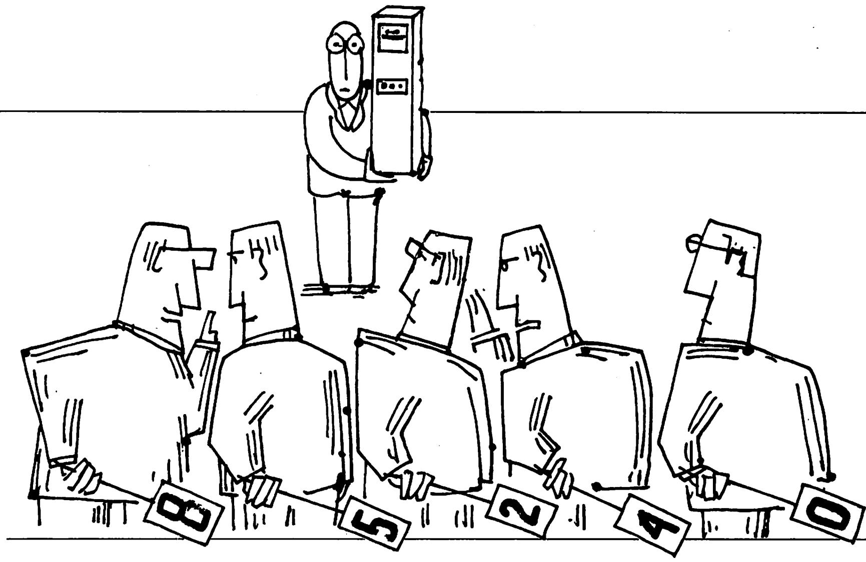

ILLUSTRATION • MACIEK ALBRECHT

Most of us who observe IBM have spent the last 12 months pondering the future of the RT PC. We have wondered if it would be a success, whether it was a major machine or just something to fill a niche, whether IBM was serious about it, and whether its formidable competition in the UNIX and scientific and engineering markets would simply wipe it out. We have mulled over the expected miniaturization of the 370 family, now a fact in the form of the new 9370, and its effect on the midrange market. We have considered the possible merger of the System/36 and System/38 families into a single, more potent midrange architecture. And we have listened to each other not praising the RT, but burying it.

It may thus seem foolhardy for *PC Tech Journal* to devote so many pages in a single issue to a machine under such a cloud of suspicion, especially when it doesn't have a thing to do with Intel microprocessors or DOS. How could I allow this to happen? To be honest, I planned it that way.

Please don't get the idea that you are suddenly reading a magazine of workstations and UNIX. *PC Tech Journal* is what it always has been: a technically oriented magazine about IBM's small computers. The RT is very technical, and it is certainly small in comparison to every IBM computer except the PC family. Furthermore, we think it is a very interesting machine from many standpoints—and one in which many of you are probably interested, even if you don't plan to rush right out and buy one. I decided, therefore, that *PC Tech Journal* had to clear the air by providing an unbiased, objective view of the RT that is more trustworthy than the wailings of security analysts and IBM-authored reviews that have appeared in some other publications.

For this formidable task we turned to our two veteran consulting editors, Richard M. Foard and Thomas V. Hoffmann, whose previous writings in *PC Tech Journal* I know you have come to trust. We are grateful to IBM, which provided two of the then-scarce machines for our dissection and let us borrow them for an unprecedented length of time. Foard and Hoffmann pored over these boxes; Foard concentrated on the software while Hoffmann took a microscope to the hardware.

Their observations and conclusions are presented in a suite of five articles beginning on page 56 of this issue. I will not attempt to steal their thunder, but a number of important points can be made about the RT.

THOSE THREE LITTLE LETTERS

Senior technical editor Jim Shields, who edited the Foard/Hoffmann articles, just returned from UNIX Expo in New York City. There he found considerable interest in, and support for, the RT. The tip of the iceberg is an IBM-published software catalog listing about 100 major applications now or soon-to-be available for the RT. Most of these are, of course, applications ported from other UNIX environments, although a few came from DOS. The significance of this is not so much the number of applications but the clear indication that software vendors see value in the existence of a UNIX box sporting the letters *I-B-M.*

The rest of the iceberg is IBM itself. Here, for the first time, is a really safe UNIX buy. Those three little letters mean that some buyers might choose a UNIX environment in situations where they would not consider a VAX or a Sun or any of a myriad of UNIX computers. A paraphrase comes to mind: "You won't lose your job for buying IBM, even if it is running UNIX."

Although the price/performance ratio of the RT is questionable, a UNIX box from IBM is bound to stir interest from numerous quarters. The RT is much more useful than a low-end System/36; small businesses undoubtedly will take note. With a wide body of applications available for UNIX, corporate planners also will consider the machine, especially when departmental computing needs dictate a relatively small configuration. The scientific and engineering community will be particularly well-served because IBM has specifically targeted them with the RT. Finally, the university environment should take to the machine because of its architecture and superb memory management facilities.

THE ARCHITECTURE SHINES

The most compelling feature of the RT at the moment is its overall architecture. Foard praises the Advanced Inter-

active Executive (AIX) operating system; privately he says, "The system just feels good," even higher praise from one who has wrestled numerous UNIX implementations to the ground. The Virtual Resource Manager (VRM) is kind of a secret weapon that gives IBM great flexibility in operating system implementation. And whereas the reduced instruction set computer (RISC) architecture is interesting, the memory management unit (MMU) is what really sets the machine apart.

The heart of the RT is the VRM/MMU combination. VRM has been likened to VM on 370-architecture machines; while it bears some resemblance, it is not quite as powerful. However, VRM considerably facilitates the port of an operating system to the RT. For example, the System/36's SSP environment could be implemented over VRM with far less difficulty than it could be rewritten for the native RT architecture. VRM is powerful enough to allow dissimilar operating systems to execute simultaneously on the same machine and to support multiple RT processors in the same box. Whether IBM will exploit these potentials is unknown, but the possibilities are intriguing.

The MMU is perhaps the best memory manager available in a small machine. It allows an absolutely enormous linear program (256 *mega*bytes) which, of course, can be virtual. The virtual address space is 1 *tera*byte (240); a segmented program could access the entire virtual space. These large numbers seem to dwarf the allowable physical memory of 16MB (224).

The key to the MMU, however, is its great flexibility. The design of the MMU allows for relatively easy redesign, so that a new processor/MMU combination could do translation to even a peculiar bit width such as 28 bits, yielding 256MB of physical memory. The change in the MMU would be completely transparent to all existing software and perhaps even to AIX; VRM would require a few adjustments.

IS IT SOUP YET?

VRM and the MMU lead me to believe that there is more to the RT than IBM would have us believe. The marketing strategy so far has been to tout the machine as a wonderful system for the scientific and engineering market, an identified strategic market for IBM (see "AT vs RT," Directions, Will Fastie, April 1986, p. 7). To judge by reactions in the press, nobody believes the "wonderful" part. The problem is mostly the delivered performance. At about 2 million instructions per second (MIPS), most think the machine is underpowered and overpriced when compared to the typical Sun workstation. The question of graphics also must be considered; although the display resolution is acceptable, high-performance graphics require the addition of an expensive 5080 graphics workstation.

We know from sources close to IBM that the RT is designed for a processor rate four times as fast as the current models, or about 8 MIPS. I felt certain that the rate would have been quickly increased to at least 4 MIPS, if for no other reason than to quell the speed objections, but IBM's recent announcements for the RT offered no base improvement in CPU performance.

The question I keep asking myself is, "Does IBM care?" I think not, because I view the machine not as IBM's entrée into the technical market but as a new architectural generation. Consider this scenario: suppose YCC (Your Computer Company) has developed a new architecture that is different from all your previous architectures. How would you test it? How could you find out what the potential market acceptance might be? How could you get third-party developers to take it seriously and to develop much-needed applications and add-on hardware?

Suppose you introduced this machine in disguise, saying, "Here's our nifty new machine for this tiny niche market," then asking, "How do you like it?," all the time keeping the price high and the performance relatively low. What is the advantage to YCC? Simple: this strategy keeps the number of machines in the field low and at the same time limits the distribution in the early days to developers, exactly the folks you want to have wringing the thing out!

These technical types then feed back tons of helpful information (in the form of complaints and gripes, of course) that can be used to adjust the machine as needed. Once tuned, you can release the set of machines you *really* want to sell, including smaller, larger, cheaper, and more expensive versions. Maybe you can release ported versions of older operating systems. Maybe you even can release some of your better and more popular office system products, freshly ported to bigger-better-faster-cheaper computers than you could previously offer.

Is this what IBM is doing? Beats me. I just see two points. First, I agree that the RT makes little sense in its identified target market. Second, it is a superbly architected system.

It's hard for me to believe that IBM would leave such craftsmanship just lying around.

RT ENHANCEMENTS

Since we began preparing our review of the RT PC, IBM introduced a new model and reduced prices for existing models. The minimum configuration of the new desktop Model 15 provides twice the internal memory (2MB) and nearly double the disk storage capacity (70MB) of the current Model 10. The Model 15 has a single-unit price of $10,050. New prices and old prices (given in parentheses) for current models are as follows: Model 10, $7,900 ($11,700); Model 20, $11,900 ($14,945); Model 25, $14,050 ($17,940); and Model A25, $15,620 ($19,510). A 4MB memory card ($4,300) that provides a maximum of 8MB of system memory is also now available for every model.

In addition, IBM has announced an Advanced Floating-Point Accelerator card ($1,995), which will perform floating-point calculations nearly three times faster than is currently possible, and a Small Computer Systems Interface adapter card ($1,080), which can support up to seven 200MB or 400MB IBM 9332 external disk drives. These cards will be made available in the second quarter of 1987, along with the IBM RT PC Computer-integrated Electrical Design Series/Design Simulation, which are five circuit design programs, ranging in price from $10,000 to $20,000.

Products announced for March 1987 delivery include the IBM RT PC Host Interface Adapter ($1,795), Workstation Host Interface Program ($995), and four host communications packages ($995 to $1,195), as well as new versions of the AIX operating system (upgrade from 1.1 to 2.1, $395), VRM (upgrade from 1.1 to 2.1, $100), SQL/RT Data Base (upgrade for 1.1 to 2.1, $200), and the IBM RT PC VS Pascal Compiler Version 1 ($1,000). The one-time license charges for AIX and VRM were also decreased from $3,400 to $2,295 and from $1,000 to $895, respectively.

—*JS*

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- Operating systems MS-DOS, PC-DOS, UNIX, XENIX, SCO XENIX, UNOS, ULTRIX, VMS
- C compilers: Lattice, Microsoft, DeSmet, Aztec, Computer Innovations, XENIX and UNIX

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*The benchmark procedure was adapted from "Benchmarking Database Systems: A Systematic Approach" by Bitton, DeWitt and Turbyfill, December 1983.

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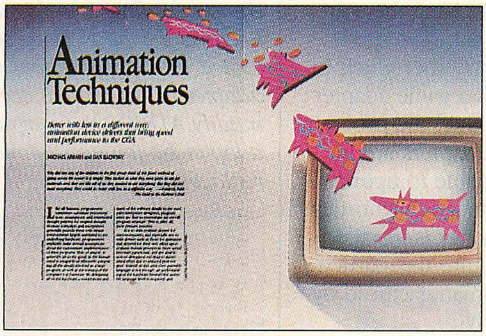

ANIMATED EXCHANGE

In their article "Animation Techniques" (July 1986, p. 46), Michael Abrash and Dan Illowsky dismiss C as too slow for realtime graphic drivers for microcomputers. My own experience in developing high-performance graphic drivers (in various languages) suggests that C is capable of performance that is far better than the authors claim. Although the authors do note that Microsoft C (version 3.0) can access display memory directly from small model programs, they fail to note other capabilities of this compiler that could be used to improve graphics performance.

If the width of an object is known at compile time, **structure assignment** statements could be used to generate in-line repeated **move string** instructions that are comparable to assembly language. This would require separate drivers for different object widths, not unreasonable, especially since the faster **move string word** instructions would be used automatically where appropriate. With separate drivers for different shapes (width and height), performance could be improved even more.

Although the authors claim that none of their more advanced techniques can be used in C, precalculation, table look-up, move string, and in-line coding all can be used to boost performance in C just as in assembly language. **Switch** statements can be used to implement jump tables. Surely a C program could be written that would be many times faster than the one shown in listing 2. It would have been instructive had the authors attempted it. Perhaps in their enthusiasm for assembly language they failed to question their own assumptions.

Of course, even the best C program can be outperformed by a carefully coded assembly language equivalent. Although for some application the difference may be crucial, for many others it will be insignificant. An optimal program is rarely necessary (and even more rarely achieved). Consequently, I normally code and debug a new application entirely in C. I rewrite critical routines in assembly language only if I first have failed to wring adequate performance from C. However, I find that by concentrating on overall program structure, I rarely need to.

John Navas II
Foster City, CA

"Animation Techniques" and "Software Sprites" (Michael Abrash and Dan Illowsky, August 1986, p. 125) remind me of similar articles I read back in 1979, although those were written with the Apple II in mind.

The authors make much of the fact that the PC is not a game machine and does not contain any specialized animation hardware. Neither does the Apple II, which has been ridiculed for years by the PC community as "only a game machine." In fact, the PC is easier to program for animation because the 8088 is a far more powerful processor than the 6502, and the memory-mapping scheme of the CGA is simpler than the scheme used by the Apple II. There is no excuse for the kind of poor animation that a lot of PC games exhibit. Commercial Apple games today do not contain XOR color interaction, byte fringing, heavy flickering, or non-overlapping objects common in PC games.

The authors also explain that structured programming, top-down design, and other high-level programming techniques must be ignored when it comes to animation. This is because they cannot provide the kind of intimate, cycle-counted code that is required to wring the last bit of performance out of unfriendly hardware.

Apple programmers have known for years how to write high-speed animation and sprite drivers without the assistance of hardware. The PC world is just now beginning to duplicate some of those techniques. As the cost of PC clones drops to below that of an Apple IIe, and thus enter the home computer market, games will be more viable for the PC. High-speed animation will become even more necessary for the PC to remain competitive game-wise, especially with Atari's 520ST and Commodore's Amiga out there.

Bruce Morgan
RM Software
Palo Alto, CA

No one approach to animation programming is the correct one. In general, a programmer should use the language and approach with which he is most productive, as long as it does the job. Our articles specifically addressed applications in which nothing less than the fastest possible code would perform adequately; they were not meant as part of a general debate about the relative worth of assembly language and high-level languages. Mr. Navas acknowledges that the best assembly language code outperforms the best C code, and we said in the article, "optimal realtime drivers must be written in assembly language." In less demanding applications, C (or any of several languages) could serve as well. We certainly agree that C provides a more productive environment for most programmers.

We would like to address a few technical points in Mr. Navas's letter. The code generated by Microsoft C 4.0 for a structure copy into a far segment is not nearly as compact as the assembly language code in our drivers, by a ratio of 19:6. This greater size, along with more frequent memory access, makes such C code bulkier and slower than our assembly language routines. In addition, C does not lend itself to in-line code, lacking the equivalent of the REPT pseudo-op. It is difficult to see how ***switch*** *could be implemented as a jump table, since case values are not required to form a consecutive set.*

This discussion misses a more fundamental point, however. The advantage to coding high-performance animation routines using machine-dependent, nonintuitive, slower C code rather than assembly language is unclear. Is it really easier to develop drivers in C using techniques such as using structures to force repeat string moves than it is to write code in assembly language using instructions such as REP MOVSW? Is the resulting code any more portable or understandable? We certainly agree that a C program could indeed be written that would be many times faster than our sample C driver. However, understanding the compiler's code generation and the use of C in unusual ways would be required, negating much of the benefit of using C. Moreover, the final code still would be significantly slower and bulkier than well-written assembly language drivers. We see no advantage to using C in such a case.

Currently our primary development language is Microsoft C 4.0, and we are quite impressed with the quality of code it generates. Nevertheless, when we need the fastest, smallest possible code—optimal code—assembly language is clearly the only choice.

Mr. Morgan's statement that superior animation techniques have been known in the Apple II world for years is quite true, but let's not forget that the Apple II market was and is a far more profitable arena for animation than the IBM PC market, so programmers have more incentive to develop excellent animation code. By the way, although an 8088 running at 5 MHz is generally much more powerful than an 6502 running at 1 MHz, animation performance is the product of many factors, including bit-map size, video wait states, instruction mix, prefetching, and available hardware tricks, as well as general processor power. Surprisingly, our extensive experience with both the Apple II and the PC indicates that the two perform at pretty much the same level with regard to animation.

—Michael Abrash
Dan Illowsky

THE SHADOW OF A DOUBT

I am writing regarding the introductory article on AT compatibles, "Out from the Shadow of IBM..." in the August 1986 issue (Steven Armbrust, Ted Forgeron, and Paul Pierce, p. 52).

Upon compiling (with Turbo Pascal version 3.0) and running the program ATBIOS.PAS (listing 1, p. 60) on an IBM PC/AT (with ROM BIOS dated 6/10/85), the field for the copyright statement printed ????? instead of giving the software copyright statement.

I also discovered another glitch in this program: although a game adapter is installed in my machine, the program reports that no game adapters are installed. I have been unable to figure this out since the advanced diagnostics shows that a game adapter is installed and programs that require this particular adapter—which is manufactured by IBM—function properly.

Richard H. Shores
Cumberland Museum and Science Center
Nashville, TN

Thank you for pointing out these two weaknesses in ATBIOS. We have modified the program to correct both of the problems that you mentioned and to add a new feature. The revised version of ATBIOS (version 1.01) is now available on PCTECHLine.

First, the problem with ????? instead of the copyright statement on 30MB IBM PC/ATs has to do with control characters located in the range of addresses displayed starting at F000:E000. The fix to ATBIOS is to filter out nonalphanumeric characters and display them as periods, much the way DEBUG handles unprintable characters in hexadecimal or ASCII memory displays. To fix the problem in your copy of ATBIOS.PAS, replace these lines:

```
write('Copyright Statement is ') ;
window(40,6,80,7);
gotoxy(1,1);
write(copyright) ;
window(1,1,80,25) ;
gotoxy(1,8);
```

with the following code:

```
write('Copyright Statement is') ;
write('                    ') ;
FOR i := 1 TO 80 DO
  BEGIN
    IF (copyright[i] < ' ')
    OR (copyright[i] > '~') THEN
      write('.')
    ELSE
      write(copyright[i]) ;
    IF i = 40 THEN
      BEGIN
        writeln ;
        write('                    ') ;
        write('                          ') ;
      END ;
  END ;
writeln ;
```

Second, the problem with detecting the IBM Game Adapter has to do with an incompatibility of the AT itself. On the AT, the game adapter bit in the equipment flags word is never set. Because this bit is never set, ATBIOS is fooled into thinking that the game adapter is not present even if it is. To modify ATBIOS to interpret the game adapter bit for non-AT machines only, replace these lines:

```
write('Game Adapter Present') ;
write('                    ') ;
if (equip_flag and game_mask) <> 0
then writeln('YES')
else writeln('NO');
```

with the following code:

```
IF machine_id <> at_id THEN
  BEGIN
    write('Game Adapter Present') ;
    write('                    ') ;
   IF (equip_flag AND game_mask)
   <> 0 THEN writeln('YES')
    ELSE
      writeln('NO') ;
  END ;
```

Finally, we have added a new feature to ATBIOS. It now supports I/O redirection so that a user can redirect its output to a file or printer. To enable I/O redirection, add the line:

{$P512}

anywhere before the first line of source code in ATBIOS.PAS.

—Ted Forgeron

FAULTY CONNECTION

At first glance the product review in "Emulating the 3278" by Roger Addelson, (February 1986, p. 48) appeared to be something micro/mainframe users have long awaited. After reading the article, however, it is easy to understand why no other major trade publication has undertaken the task of evaluating 3270 emulation products. Apparently, very few authors, including Mr. Addelson, are sufficiently knowledgeable about IBM mainframes and data communications, as well as microcomputers, to conduct such a review.

Mr. Addelson's understanding of 3270 network configuration options, although somewhat correct, needs much refinement. He identifies three categories of connections: dial-in, leased line, and direct-channel connect. Dial-in is used to refer to connection over the telephone company's switched network. Leased line is the common term for a connection via a nonswitched or dedicated phone line. (Our local phone company uses the term "private line" to refer to a nonswitched line, insisting

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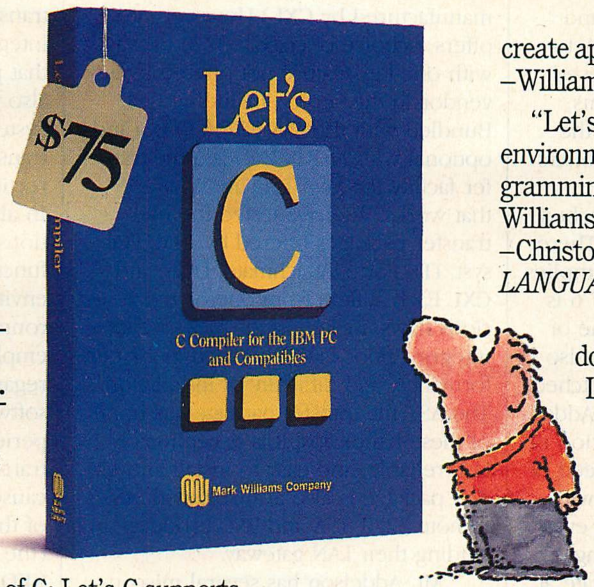

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Let's C Benchmark Done on an IBM-PC/XT, no 8087. Program: Floating Point from BYTE, August, 1983.

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that all of their lines, switched or nonswitched, are leased lines.) From the discussion on connection options and figures 1 and 2, we are led to believe that 3276 emulation on a PC, whether a single display cluster or as a gateway in a LAN, works only with modems and the switched telephone network. Actually, connection also may be achieved via nonswitched lines with modems, and through direct connection to the 3704/05/25 communications controllers without modems.

Figure 3 shows a channel-attached 3276 control unit display station. There is no such thing. The figure also implies that remote attachment of a 3274/76 is possible only through a leased line or T1 carrier, when in fact a 3274/76 also can be connected through the switched telephone network (dial-up). Mr. Addelson states that dial-in 3276 emulation is limited to a maximum transfer speed of 2400 bits per second (bps), even with recently released modems. Today even protocol converters communicating over asynchronous links can operate at speeds of up to 9600 bps, and dial-in operation with 9600-bps synchronous modems is not uncommon.

Missing from the field of vendors evaluated is AST Research. Better known for its multifunction boards, AST has made significant inroads in the micro-to-mainframe arena. The explanation for the omission is that AST is not the original manufacturer of its coaxial board. (The board was originally designed and manufactured by CXI.) However, AST offers a choice of coaxial 3270 packages with one key feature not offered by any vendor in the survey, including CXI. Bundled with the AST-3270/COAX (and optional with AST-PCOX) is a file-transfer facility for MVS/TSO and VM/CMS that works. We have tested the file-transfer packages offered by IBM, Persyst, ITI, Forte, Attachmate, DCA, and CXI. Each suffers from one or more serious flaws, including the lack of data integrity, poor fault tolerance, poor performance, and difficulty of installation. The AST file-transfer package has none of these handicaps; it is exceptionally fast, reliable, and easy to install and use. The package is also available with AST's remote 3270 SNA and BSC products, including their LAN gateway.

Mr. Addelson has several misconceptions about PC-based, editor-oriented, file-transfer packages. One misconception is that all such packages are inherently slow, due to the technical limitations of using a host editor. The AST file-transfer package dispels this myth completely. Based on the TSO and CMS host editors, both versions deliver performance that rivals the best mainframe-based packages.

Another misconception is that file-transfer packages cannot guarantee data integrity without mainframe software that performs validity checking. This is also wrong. According to the ISO Open Systems Interconnection model, data transmission error detection and correction is a function of the Link layer. In all IBM synchronous communications, 3270 networks included, this function is provided by SDLC in SNA environments or BSC in non-SNA environments. Hence, this error detection is employed by these file-transfer products regardless of the utilization of any host software. Any data-integrity problems experienced with host editor-based, file-transfer software is most likely to be caused by an incorrect implementation of the Application layer of the protocol (the interface to TSO EDIT or CMS XEDIT) in the PC software. The AST file transfer does an excellent job of maintaining data integrity, whereas some host-based packages (such as those provided by IBM and DCA) are prone to adding bytes to the end of files.

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*as reported in Micro Cornucopia, August-September 1985. Turbo Pascal is a registered trademark of Borland International.

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Finally, Mr. Addelson discusses the limitations surrounding the micro-to-mainframe transfer of PC binary files. He states that the transmission problem is a result of the inability of the mainframe editors to handle 8-bit characters; they use 7 bits to represent the character and the high-order bit is usurped in a parity-checking scheme. This, however, is incorrect. Although mainframe editors and utilities have various restrictions, the data transparency limitation is a function of the 3270 data stream protocol and the 3270 I/O interface code that is used.

The lack of transparency of the 3270 data stream protocol limits the number of codes available to represent data. Because binary files contain codes in the complete range of the 256 possible values, conflicts exist where data values overlap with 3270 orders. In addition, code assignments not defined by the I/O interface code being employed (selected when ordering or installing the 3270 control unit) cannot be transmitted. A common method of allowing the exchange of binary data within a micro-to-mainframe environment is to encode the file, prior to transmission, to a format permitting data transparency. One efficient encoding scheme utilizes a 3:4 mapping, where three bytes of binary data are mapped to four bytes of character data for processing. This mapping is much more efficient than the 1:2 scheme employed by the packages that were evaluated.

Stan H. King, executive vice president
Warren A. Mackensen, president
Mackensen Corporation
Santa Monica, CA

The points regarding dial-in, leased lines, and direct connect are technically correct, but not critical to the points being discussed in the article. The point of the discussion of access options in the article was to give a brief review of the common methods to achieve 3270 communications. The use of 9600 asynchronous communications over dial-up lines is both uncommon for a single terminal 3276 (or PC emulating a 3276) and extremely expensive. It is more common for a 3274/76 with multiple terminals attached (a configuration not relevant to the discussion because the article dealt with options for single PCs, not LANs). The diagrams were meant to show the three types of 3270 communication schemes. Figure 3 shows the options with a cluster controller. We tried to show both channel connection and 3705/25 connection in one diagram. Because of this, the diagram (not the text of the article), implied 3276 channel connection. This is technically incorrect; only certain models of the 3274 can be channel-connected. The assertion in the letter that 3276s can be connected directly to a communications controller is correct, however null modems are necessary.

Because the AST board was not evaluated, I cannot comment at present on the assertions regarding the superiority of the product. Based upon an examination of the products evaluated, and my benchmark tests, I stand by my conclusions regarding editor-based file-transfer packages.

I do not agree with some of the statements in this letter regarding the SNA protocol. Messrs. King and Mackensen imply that SNA follows the ISO Open Systems Interconnection model. Although a number of layers in SNA parallel ISO—they are quite similar in many regards—SNA never proclaims to follow the ISO protocol; it is a protocol

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unto itself. The point they seem to be making, however, is that the application need not perform integrity checks because they are handled in the Link layer. This does not assure adequate data integrity for file transfer. Prudent application programmers commonly include check-digits, CRC, or other integrity checks in their software, especially if it involves file transfer.

Messrs. King and Mackensen assert that the discussion of the file-transfer's 7-bit limitation is incorrect. Their information on the lack of transparency in the 3270 protocol is certainly relevant; however, TSO EDIT and XEDIT's character-handling limitations are also a constraining factor. The assertion that 3:4 mapping is more efficient than 1:2 mapping may be correct, but none of the file-transfer packages reviewed in the article uses that scheme.

Even 3:4 mapping with an editor-based file-transfer package does not allow real data transparency. A mainframe-based program must remap the four bytes back to the original three, a function not performed by the mainframe editors. The mapped file on the mainframe is useless unless downloaded back to the PC and translated to the correct form. As stated in the article, this is only useful when using the mainframe to archive PC data. The data cannot be downloaded to the PC that is using other file-transfer packages because the other packages do not include the same remapping scheme.

—Roger Addelson

Regarding the AST 3278/79 package not being evaluated, PC Tech Journal *chose in this case to review equipment from original manufacturers in order to avoid duplication. AST was a VAR (value-added reseller), adding only its own file-transfer routines. In light of the information provided by Messrs. King and Mackensen, the AST package is being considered for review.*

—JS

ERRATA

Regarding "The EGA Spectrum" (John T. Cockerham, October 1986, p.48), please note the following corrections:

On page 50 in the first column, the phrase that reads "(or 3D4 and 3D5 at the alternate I/O address)" should say "(or 3D4 and 3D5 if the EGA is configured to be a Monochrome Display)". The implication is that the other I/O addresses are for the second EGA card. This is not so, as explained in the succeeding paragraph on that page.

In the caption for table 1 (p. 50), the first sentence should read, "The data register in all cases is 3x5."

In connection with the discussion that begins on page 61, the EGATEST program requires an auxiliary file, OTHRFONT.DAT, in order to run. This file contains a modified font so that the user of EGATEST will have the ability to see the font cycling. (OTHRFONT.DAT is available on PCTECHline.

On page 63, in the first paragraph at the top of column three, the sentence that begins, "These numbers..." should read, "These numbers will *not* be shared by the non-C&T boards to be reviewed next month. The C&T boards' BIOS call timings, however, varied widely from a reasonable 27.4 seconds to an agonizing 64.3 seconds."

Also note that the routine in LOWEGA (listing 2A) called WaitForVerticalRetrace actually waits for the Vertical Display End signal. The name was chosen because it implies what the adapter is really doing.

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Greenleaf Communications *by Greenleaf*	185	**139**
PTel *by Phoenix, Binary File Communicator*	195	**149**
Software Horizons Pack 3	149	**119**
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Blaise C Tools Plus	175	**149**
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Lattice now delivers smaller .EXE files, boasts very fast link times and a more efficient aliasing algorithm. New options generate code to use 80186 and 80286 features; 8087 of course sensed and utilized. Lattice has enjoyed pre-eminence so long that developers have created far more snap-on tools for Lattice C than any other compiler. William Hunt's *PC Tech Journal* review of 12 compilers awarded Lattice the only "very good" rating for add-on library availability.

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MICROSOFT LANGUAGES NEWSLETTER Vol. 1, No. 12

News about the Microsoft Language Family

Debugging with Two Monitors Simultaneously Using the Microsoft® CodeView™ Debugger.

The Microsoft CodeView, the revolutionary window-oriented symbolic debugger in Microsoft C Compiler Version 4.0, is a powerful tool. One of its numerous capabilities is the versatile way it enables programmers to view their code's output on the default monitor and video adapter while debugging on another monitor and video adapter. This is especially helpful for graphical applications. For example, if you have both a Color Graphics Adapter (CGA) and a Monochrome Adapter in the same system, you might want to set up the CGA as the default adapter. You could then debug a graphics program with the graphics display appearing on the graphics monitor and the debugging display appearing on the monochrome monitor. This feature is evoked by typing:

CV/2 ***program name***

If you only have one graphic adapter and monitor in your system, you may use the screen swapping (/S) or flipping (/F) options to view your output while debugging with CodeView.

Finding Null Pointer Assignments with Microsoft CodeView.

When a value is assigned to an uninitialized pointer in C, the Microsoft C runtime code displays:

error 2001: Null pointer assignment

This is because it is impossible to tell at runtime that such an operation has occurred (the runtime routine "_nullcheck( )" checks the first 54 bytes of the data segment to see if they have been changed when the program terminates). With Microsoft CodeView, this problem can be easily discovered. Debug your program with Microsoft CodeView and execute the program up to "main( )" to set the DS register to the program's data segment. Now set a tracepoint on the first byte of the data segment using the command "TPB 0" (the pull-down menu can also be used). Now execute the program using the "go" command. When the program attempts to use an uninitialized pointer, thus writing to location 0, Microsoft CodeView will halt execution of the program just after the offending instruction. This operation can be made even faster using debugging hardware compatible with the Microsoft CodeView debugger.

Debugging Assembly Language Programs with Microsoft CodeView.

Microsoft CodeView has special features for the assembly language programmer. The radix command allows the user to set the default input and output radix so that assembly language programmers can use hex numbers just like the popular Microsoft SYMDEB debugger and DEBUG. To switch to hex simply type:

n16

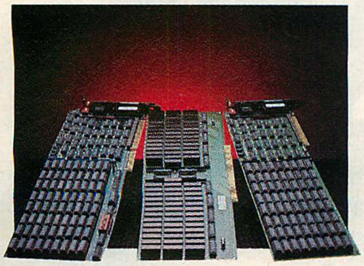
In addition, the assembly and register displays allow viewing of code at the machine level. If you're debugging Microsoft C code, the assembly display will also show local symbols in the disassembly listing, so "MOV SI, [BP-4]" might be displayed as "MOV i, [count]." A unique backward-scroll mechanism allows you to quickly scroll backward through disassembled code.

For more information on the products and features discussed in the Newsletter,
write to: Microsoft Languages Newsletter
16011 NE 36th Way, Box 97017, Redmond, WA 98073-9717.
Or phone:
(800) 426-9400. In Washington State and Alaska, call (206) 882-8088. In Canada, call (416) 673-7638.

Latest DOS Versions:

Microsoft C Compiler	4.00
Microsoft COBOL	2.10
Microsoft FORTRAN	3.31
Microsoft Macro Assembler	4.00
Microsoft Pascal	3.31
Microsoft QuickBASIC	2.00

Look for the Microsoft Languages Newsletter every month in this publication.



The JRAM Family

This series of add-on boards from Tall Tree Systems consistently incorporates a standard high-capacity memory with the latest functional capabilities.

There is more to memory than simply remembering. This is the principle upon which Tall Tree Systems was founded and continues to follow. While most vendors of PC add-on products have looked upon memory as simply one of four functions on a four-function board, Tall Tree has seen it as a foundation upon which to build entirely new functions. Since the introduction of the first JRAM in February 1982, this family of memory boards has been first or nearly first in providing the PC with RAM-disk function, print-spooler function, bank-switching, inboard laser printer buffering, and most recently, 8MB RAM support for the RT PC. In recognition of the engineering expertise and systems vision represented in these products, *PC Tech Journal* has named Tall Tree Systems' JRAM family of memory boards its collective Product of the Month for December 1986.

Tall Tree founder John Henderson knew from his long experience in the electronics industry that memory prices would drop severely as chip volume shot into the hundreds of millions, so all of his boards are designed for very high memory capacity, even if all sockets would not be filled immediately. The original JRAM's support of up to 2MB of RAM on the bus of a PC required one innovation—bank-switching—and suggested another—the high-capacity RAM disk. Tall Tree's JetDrive software was the first commercial RAM disk for the PC. In speeding up the edit/compile/link cycle by a factor of 10, it changed the way many software developers approached their work.

JRAM-2, released in March 1984, incorporated the basic design of JRAM, along with connectors for daughterboards containing serial and parallel ports and a clock/calendar. JRAM-AT, which was released in February 1985, provided a choice of JRAM bank-switched memory or 16-bit extended memory for the PC/AT.

The JRAM boards had been bank-switching for more than three years when the LIM EMS (Lotus/Intel/Microsoft expanded memory specification) was announced with fanfare in late April 1985. Not quite two months later, JRAM-3 was shipped, supporting both the original JRAM bank-switching specification and the new LIM EMS specifically. JRAM-3 was migrated to the AT as JRAM-3 AT at the end of 1985. It provided a choice of JRAM bank-switching, LIM EMS, or AT extended memory.

Earlier this year, Tall Tree began shipping a small daughterboard, called JLaser, for the JRAM-3 boards. JLaser provides an entirely new use for EMS RAM—as bit-mapped storage for laser printers. JLaser connects to the xerographic engine within popular laser printers (Canon and Ricoh currently; more are under development) and allows application programs to build a 300-dpi (dots per inch), bit-mapped page image within EMS RAM. On command, JLaser transfers the image to the xerographic engine as quickly as it can move paper past the photosensitive drum, without the speed bottleneck inherent in moving huge bit-mapped buffers over 9600-baud serial cables. The printer's OEM controller is neither removed nor disabled except when JLaser is printing. When not printing or storing images to be printed, the JRAM-3 expanded memory is available for use with RAM disks and EMS-knowledgeable applications such as Lotus 1-2-3.

In addition to providing 300-dpi, full-page graphics to low-end laser printers, a recent enhancement to JLaser takes control of the rate at which the laser scans the image onto the drum, allowing up to 600-dpi resolution in the horizontal dimension. (Vertical resolution is limited by the speed at which paper moves through the printer.) Aliasing in the horizontal dimension, particularly visible in line graphics output, is greatly reduced by this technique.

JLaser's third major feature is a port for the Canon scanner, allowing JRAM expanded memory to serve as a buffer for images scanned from paper documents. Software support for JLaser currently includes ZSoft's PC Paintbrush and PC Presentation, Media Cybernetics' Halo and Halo DPE desktop publishing editor, SoftCraft's Fancy Font, Personal T_EX's PC T_EX, Data Tranforms' Printrix and Fontrix, and Xerox's Ventura Publisher desktop publishing system.

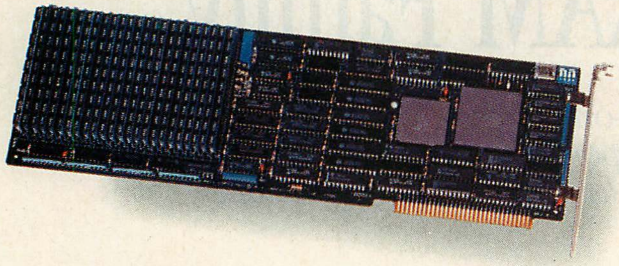
The most recent addition to Tall Tree's JRAM family, JRAM-RT, is the first third-party memory product for IBM's RT PC, offering 8MB of RAM for $3,995—one-third the price for a similar memory system from IBM. JRAM-RT is one of the first PC products to incorporate 1-megabit DRAMs, permitting 8MB to fit uncrowded on a single board without daughterboards. JRAM-RT appeared quickly indeed, especially considering that Tall Tree had no advance information on the RT PC.

John Henderson has identified high-resolution image processing and printing as areas of future development for Tall Tree Systems. Because memory prices have fallen, his belief is that high-resolution laser printers can only follow. Other directions for the JRAM family are not as clear. It is a fair guess, however, that as new bus structures appear, such as the 32-bit PCET (Personal Computer Extended Technology) specification now emerging from committee, a JRAM board will quickly follow, bringing with it memory that remembers . . . and then some.

JRAM-2: $199; JRAM-AT: $269; JRAM-3: $269; JRAM-3 AT: $349; JLaser: price varies by configuration; JRAM-RT: $3,995
Tall Tree Systems
1120 San Antonio Road
Palo Alto, CA 94303
415/964-1980

CIRCLE 345 ON READER SERVICE CARD

Hardware, software, and other developments for the IBM PC family



386 HummingBoard by Gold Hill Computers and AI Architects

Compaq Deskpro 386

FROM IBM

A faster, more powerful PC/XT, featuring increased memory and a 6-MHz Intel 80286 microprocessor, has been introduced by **IBM Corporation**. The **IBM Personal Computer XT Model 286** (XT-286) comes with 640KB of zero-wait-state memory, with various expansion options to increase memory up to 12.6MB. Features include a half-height, 1.2MB, 5¼-inch, double-sided diskette drive; a 20MB fixed-disk drive with an average access time of 85 milliseconds; a serial/parallel adapter card; five 16-bit and three 8-bit I/O expansion slots; clock/calendar; and the IBM Enhanced Personal Computer Keyboard. XT-286, $3,995. Optional second diskette drive in three half-height, double-sided configurations: 3½-inch with 720KB internal, $190 (also available for PC/AT Models 319 and 339); 5¼-inch with 1.2MB, $275; 5¼-inch with 360KB, $225.

IBM also announced an enhancement to the two 20MB fixed-disk drive models of the PC/XT (Models 088 and 089), increasing the standard system board memory from 512KB to 640KB with no change in price.

A new software package, **SY-TOS**, facilitates tape backup for the PC. SY-TOS is designed to work with the IBM 6157 Streaming Tape Drive. The program supports file, partition, or entire disk backup, and restore. $70. *IBM Corporation, 100 Summit Avenue, Montvale, NJ 07645; contact the local IBM dealer, 800/426-2468*

CIRCLE 301 ON READER SERVICE CARD

The **IBM 3162 display station** is a general-purpose terminal for computers using the ASCII communications protocol. The 3162 can attach to the IBM Series/1, IBM System/88, IBM PC, the IBM RT PC, and most non-IBM host computers. The 3162's 14-inch (diagonal) screen, available in green or amber, offers 24 or 28 lines per screen with 80 or 132 characters per line, for a display of as many as 3,696 characters. It is designed with tilt/swivel displays and etched screens. Features include definable function keys, extended menu setup, split screens, and smooth scrolling in two speeds. $645.

The **Realtime Interface Coprocessor** (ARTIC) is designed as a single-slot multiple device interface subsystem for IBM Industrial Computers and PCs. This coprocessor feature is based on the Intel 80186 microprocessor and includes the Realtime Control Program microcode. The microcode provides the user with a realtime, multitasking operation environment for supporting industrial applications running on the coprocessor. The coprocessor can be attached to industrial equipment and may be programmed to support a variety of protocols. 128KB version, $1,295; 512KB version, $1,695.

Also introduced are several software products for use with the Realtime Interface Coprocessor. The **Communications Subsystem 1.1** is a software communications facility for routing messages between a PC and Realtime Interface Coprocessors. $475.

The **Realtime Control Program DOS Support** is a set of DOS-compatible program modules that support the IBM Industrial Computer and PC applications for one or multiple Realtime Interface Coprocessors. $80.

The **Realtime Interface Coprocessor Developer's Kit** contains program support that allows the user to develop-applications using a high-level language. It has a program debugger for programs executing on the Realtime Interface Coprocessor and a dump formatter for printing files. $1,850. *IBM Corporation, Information Systems Group, 900 King Street, Rye Brook, NY 10573; contact the local IBM dealer, 800/426-2468*

CIRCLE 302 ON READER SERVICE CARD

HARDWARE

Compaq Computer Corporation has announced the **Compaq Deskpro 386**, based on Intel's 16-MHz, 32-bit 80386 microprocessor. Model 40 includes 1MB RAM, a 40MB fixed-disk drive with an average access time of 28 milliseconds (ms), 1.2MB diskette drive, Compaq Expanded Memory Manager (CEMM), realtime clock, security key lock, multipurpose controller board, 80287 coprocessor socket, standard interfaces for parallel printer and serial/asynchronous communications, and the Compaq Enhanced Keyboard. Three available expansion slots accept 8/16-bit boards and three others accept 8-bit boards. Model 70 includes everything offered by Model 40 except that it has a 70MB fixed-disk drive with an average access time of 35 ms; Model 130 has a 130MB fixed-disk drive with an average access time of 19 ms. Both of these models have two available slots for 8/16-bit boards and three for 8-bit boards.

Each model is expandable to 14MB of RAM with Compaq memory upgrade kits and expansion boards, and to 10MB of 32-bit RAM without occupying an expansion slot. Monitor options include the Compaq Color Monitor and Compaq Enhanced Color Graphics Board (compatible with the IBM EGA); or Compaq Dual-mode Monitor and Compaq Video Display Controller Board. Model 40, $6,499; Model 70, $7,299; Model 130, $8,799; Compaq Color Monitor, $799; Compaq Enhanced Color Graphics Board, $599; Dual-mode Monitor, $255; Video Display Controller, $199. *Compaq Computer Corporation, 20555 FM 149, Houston, TX 77070; 713/370-0670*

CIRCLE 303 ON READER SERVICE CARD

Gold Hill Computers, Inc. and **AI Architects, Inc.** have announced an 80386-based, plug-in board with mem-

Sperry PC/IT (left) and a new smaller version, PC/microIT

ory for the PC, PC/XT, and PC/AT. The **386 HummingBoard** runs the Golden Common LISP (GCLISP) Developer. Based on the 32-bit Intel 80386 running at 16 MHz, it runs large LISP applications quickly. Directly addressable, on-board memory is expandable to 24MB with one-megabit DRAMs (up to 6MB with 256 DRAMs). With 6MB RAM and GCLISP 386 Developer, $7,000.
Gold Hill Computers, Inc., 163 Harvard Street, Cambridge, MA 02139; 617/492-2071
CIRCLE 307 ON READER SERVICE CARD
AI Architects, Inc., One Kendall Square, Suite 2200, Cambridge, MA 02139; 617/577-8052
CIRCLE 308 ON READER SERVICE CARD

Advanced Logic Research, Inc. has announced a line of 80386-based microcomputers. The **ALR Access 386** is available in three configurations. The basic system offers a 16-MHz clock speed, 512KB interleaved 32-bit RAM, one serial port, one parallel port, and a 1.2MB diskette drive. The enhanced monochrome system features 1,024KB RAM, 16-MHz clock speed, two serial ports, two parallel ports, 1.2MB diskette drive, 30MB hard-disk drive with an average access time of 40 milliseconds, hard-disk/diskette controller, Hercules-compatible monographics video card, and a high-resolution TTL tilt/swivel monitor. The enhanced color system contains 512KB interleaved 32-bit RAM, 16-MHz clock speed, ALR Challenger Multifunction Card with 2MB RAM expandable to 4MB, two serial ports, two parallel ports, 1.2MB diskette drive, hard-disk/diskette controller, ALR EGA Adapter Card with printer port, and 14-inch EGA/CGA monitor with tilt/swivel base. Basic system, $3,990; enhanced monochrome system, $5,890; enhanced color system, $6,949.
Advanced Logic Research, Inc., 10 Chrysler, Irvine, CA 92718; 714/581-6770
CIRCLE 304 ON READER SERVICE CARD

An 80286-based machine from **Sperry Corporation**, the **Sperry PC/microIT** has a footprint of 15 inches by 15 inches and selectable speeds of 6.0, 7.16, or 8.0 MHz. The 8.0-MHz speed can be configured with a zero- or one-wait state. Its standard 512KB memory can be increased to 1.5MB without using an expansion slot or to 3.5MB with a single card. Features include an 8-MHz Intel 80287 socket, clock/calendar with battery backup, front-mounted configuration DIP switches, parallel and serial port, dual-drive disk controller, two 8-bit and three 8/16-bit expansion slots, security key-lock switch, and switchable 135-watt power supply. Users optionally can install a 1.2MB or 360KB diskette drive plus a nonremovable 20MB hard-disk drive. Other options include a 20MB on-card hard-disk drive to allow a 20MB storage configuration with two diskettes. With 512KB, $2,345; with 512KB and a 20MB hard-disk $3,590.
Sperry Corporation, World Headquarters, P.O. Box 500, Blue Bell, PA 19424-0031; 215/542-2240
CIRCLE 310 ON READER SERVICE CARD

Intel Corporation's Personal Computer Enhancement Operation has announced the **Inboard 386/AT**, an add-in board with a 16-MHz Intel 80386 microprocessor for the PC/AT and compatibles. When control software programs become available (scheduled for mid-1987), the board will provide true multitasking and concurrent processing abilities. Inboard 386/AT is compatible with AT motherboards operating at 6, 8, and 10 MHz, and it is compatible with Intel's Above Board products. The 386/AT includes a 64KB high-speed memory cache that enhances application program performance. Extended memory to 1MB can be added to Inboard 386/AT (plus an additional 2MB with a piggyback board). The board is equipped with a socket for the 80387 numeric coprocessor. 0KB, $1,995.

Intel also has announced a bubble memory expansion board that provides up to 1MB of nonvolatile storage. The **iPCB-76 PC-Bubble Card** emulates the storage functions of a hard-disk drive. The board can withstand harsh environmental conditions, such as extreme temperatures, shock, vibration, moisture, and dust. An evaluation version of the PC-Bubble Card, the **iPCB-75,** features the company's proprietary 4-SITE software. 4-SITE enables designers to learn to program a bubble memory controller and build a prototype bubble-based system. iPCB-76 (quantities of 100) for 1MB, $1,445 each; for .5MB, $795. iPCB-75 evaluation version (single orders only) for 1MB, $945; for .5MB, $495.
Intel Corporation, Literature Dept., Suite W-316, 3065 Bowers Avenue, P.O. Box 58065, Santa Clara, CA 95052-8065; 800/548-4725
CIRCLE 306 ON READER SERVICE CARD

Okidata has entered the laser printer arena with its **Laserline 6**, which prints six pages per minute. A standard 15 resident typeset-quality fonts are included, and additional font modules are available. The Laserline 6 has a 128KB page-image buffer with an optional memory expansion cartridge of 384KB. The optional plug-in, multiuser module enables three users to share the printer. The Laserline 6 provides face-down, correct-order stacking of paper. $1,995;

Laserline 6 from Okidata

VAXmate from Digital Equipment Corporation

Okidata's first modem, the Okitel 1200

memory expansion cartridge, $399; four optional font cartridges, $149 each; multiuser module, $600. Optional personality module that provides compatibility with the HP LaserJet, $200; with the HP LaserJet Plus, $400.

Okidata's **Okitel 1200**, a 300/1200-bps (bits per second) external modem, features Automatic Adaptive Equalization (AAE), which enables the modem to look at line characteristics and automatically adjust its filters to bypass line interference. The Okitel 1200 automatically configures itself to the transmission speed of incoming calls. $499.
Okidata, 532 Fellowship Road, Mount Laurel, NJ 08054; 609/235-2600
CIRCLE 311 ON READER SERVICE CARD

Digital Equipment Corporation has introduced three major products. The **PC ALL-IN-1** is an easy-to-use MicroVAX II-based system that allows as many as 30 PCs to be part of an integrated office configuration. The **VAX/VMS Services for MS-DOS** is a software product that combines the resources of VAX/VMS and DOS into one fully networked environment by allowing VAX and MicroVAX computers to act as information servers.

PC/AT-compatible **VAXmate** is a networked personal computer specifically designed to support network group systems. VAXmate consists of a one-piece monitor/system unit with a 1.2MB 5¼-inch diskette drive, keyboard, and mouse. The VAXmate system software includes DOS 3.1 and Microsoft Windows applications interface, Microsoft Network client software, as well as Digital VT220 and VT240 terminal emulators. In addition to a built-in EtherNet transceiver, video controller, 1MB memory, communications ports, and printer ports, the base VAXmate system can accommodate an additional 2MB memory, a 300/1200/2400-bps (bits per second) modem, and a numeric coprocessor. PC-ALL-IN-1, $81,160; VAX/VMS Services for MS-DOS, $650 to $19,500 depending upon configuration; VAXmate, $4,045; software license, $250.
Digital Equipment Corporation, Maynard, MA 01754-2571; 617/897-5111
CIRCLE 309 ON READER SERVICE CARD

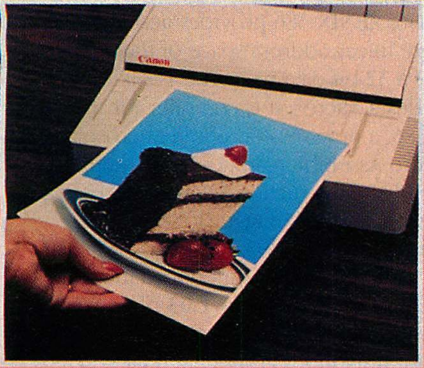
Ramtek Corporation has released the RAMTEK OWL, a system that provides high-resolution color graphics display capabilities for the PC/AT and the RT PC. The OWL features a 1,280-by-1,024 pixel, 19-inch color monitor; 60-Hz screen refresh; 4,096 colors with the ability to display 256 simultaneously; compatibility with third-party application software; single-slot connection to a host PC; an integrated display generator/monitor package; and high-performance, local graphic display list processing. $5,595.
Ramtek Corporation, 2211 Lawson Lane, Santa Clara, CA 95052-8024; 408/988-2211
CIRCLE 319 ON READER SERVICE CARD

A 19-inch, high-resolution monochrome monitor for the RT PC, designed for multiple windowing applications and desktop publishing, has been introduced by **Moniterm Corporation**. With a 1,024-by-768 display format, refreshed at 60 Hz, the **Model RT-6155** is a plug-to-plug replacement for the 15-inch IBM 6155 Extended Monochrome Graphics Display; it plugs into the IBM 4768 Display Adapter. $1,350.
Moniterm Corporation, 5740 Green Circle Drive, Minnetonka, MN 55343; 612/935-4151
CIRCLE 313 ON READER SERVICE CARD

Tall Tree Systems has taken aim at the desktop publishing industry with **JLASER PLUS**, a memory board with an interface to the Canon LBP-CX laser printer and the Canon IX-12 scanner. JLASER PLUS can triple scanning speed and increase printing speed by a factor of 50, while providing 300-dpi (dots per inch) resolution. The 2MB memory can be used as system memory, LIM EMS (Lotus/Intel/Microsoft expanded memory specification) memory in a PC/AT-type machine, RAM disk, or print spooler. For PC/XT, $599; for PC/AT, $699.
Tall Tree Systems, 1120 San Antonio Road, Palo Alto, CA 94303; 415/964-1980
CIRCLE 314 ON READER SERVICE CARD

AID/88 from **Vu-Data Corporation** provides automatic intelligent diagnostics for the PC and PC/XT system boards using the 8088 microprocessor. It is preprogrammed with 10KB of software to monitor IBM's resident diagnostics in the PC-1 (both versions), PC-2, XT and Portable PC. The firmware internal to AID/88 performs complete bus-shorted and bus-stuck (forced) testing. The **AID/PI Expansion Unit** accepts a library of plug-in assembly language programs called **PI Program Modules**. These expand the automatic intelligent diagnostics capabilities to include adapter cards and compatibles. AID/88, $2,995; AID/PI, $1,000; PI Program Modules, $250 each; eight-module set, $1,000.
Vu-Data Corporation, 9180 Brown Deer Road, San Diego, CA 92121; 619/452-7670
CIRCLE 320 ON READER SERVICE CARD

A synchronous DMA serial controller for the PC, PC/AT, and RT PC running XENIX or UNIX has been introduced by **Adax, Inc.** The **PC-SDMA** features multiple protocol control and operates on RS-232 or RS-449 standard interfaces. The PC-SDMA with RS-422 drivers and receivers can transmit as fast as 1 megabit per second. It supports multiple low-level communications protocols on XENIX, such as X.25/HDLC, IBM/SDLC, and ASYNC. Adax provides software for the X.25 protocol and for basic and standard DDN high-level protocols. $790; software, $1,500 to $2,000.
Adax, Inc., 737 Dwight Way, Berkeley, CA 94710; 415/548-7047
CIRCLE 315 ON READER SERVICE CARD



It makes desktop publishing a piece of cake!

Tall Tree Systems introduces another breakthrough in desktop publishing with JLASER PLUS. We've combined a 2 MB EMS memory board and an interface to both a Canon®-based laser printer and scanner. JLASER PLUS increases the performance of both devices and gives you a low-cost solution to the limitations you've been experiencing with them.

Furthermore, the same memory that is made available to your printer and scanner is also available for all your other conventional applications. You get system memory, expanded LIM memory, extended memory in an AT-type machine, RAM Disk and print spooler — all in a single slot!

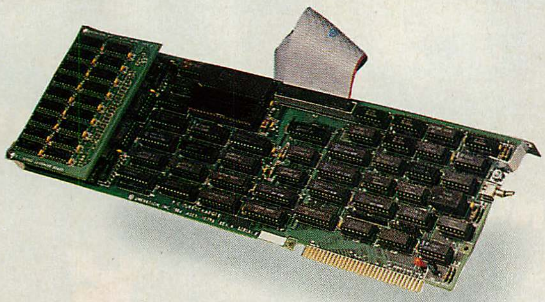
Supporting JLASER PLUS is a host of software packages, such as PC Paintbrush + from ZSoft, Dr. Halo D.P.E. from Media Cybernetics, LaserGL from Software Express, Ventura Publisher from Xerox, Page Builder from White Sciences, Le Print from Le Baugh Software, Fancy Font and Fancy Word from SoftCraft, Inc., and many more to be announced.

It takes a technological innovator like Tall Tree Systems to provide a major advancement like JLASER PLUS. And we don't stop at performance. We also deliver value, which is truly icing on the cake.

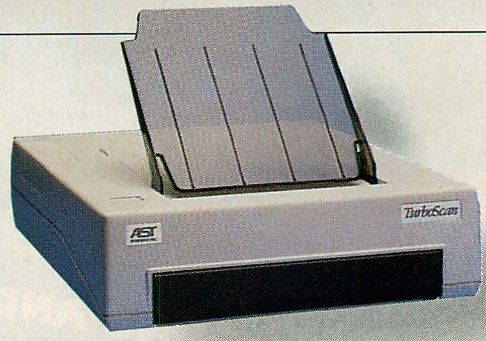
TALL TREE SYSTEMS
1120 San Antonio Road
Palo Alto, CA 94303
(415) 964-1980

CIRCLE NO. 194 ON READER SERVICE CARD

TALL TREE SYSTEMS



Dream Board from Univation



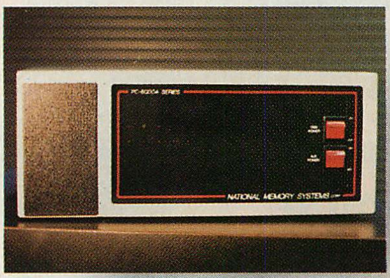
AST TurboScan, an optical page scanner

Trade Ventures International, Inc. has announced two expansion boards that address up to 15MB of RAM on a PC/AT or compatible. The **MEM-AT+** provides as much as 3MB per board; the **Multi-3 AT** provides up to 2MB in addition to two serial ports and one parallel port. These zero-wait-state memory boards can be used in combination in the same computer, filling out the base memory to 640KB and providing expanded memory or an addressable capacity of 15MB of extended memory when up to five boards are used together. These PC/XT-sized, 16-bit memory boards are produced by Elektronik Infosys of West Germany. MEM-AT+ for 0KB to 3MB, $500 to $1,495; Multi-3 AT for 0KB to 2MB, $695 to $1,395.
Trade Ventures International, Inc., 512-A Herndon Parkway, Herndon, VA 22070; 703/435-3800. European office, Blaufahnenstr. 14, CH-8001, Zurich, Switzerland; 41/1/251-7475
CIRCLE 312 ON READER SERVICE CARD

Univation's **Dream Board** offers the capabilities of a standard multifunction board, an LIM EMS board, and a system accelerator board all in one for the PC and PC/XT. The Dream Board provides two I/O ports (one serial and one parallel, or two serial), clock/calendar, system accelerator capabilities consisting of a 10-MHz Intel 8086-1 microprocessor, and expanded RAM capacity of 2MB. The board consists of three main components, a full-length primary circuit board, and two one-third-length piggyback boards; it fits into a single XT slot. A socket is provided for an optional 10-MHz Intel 8087-1 numeric coprocessor. With 512KB RAM, $795.
Univation, 1231 California Circle, Milpitas, CA 95035; 408/263-1200
CIRCLE 318 ON READER SERVICE CARD

TurboScan, an optical page scanner from **AST Research, Inc.**, can convert color or black-and-white text, handwriting, artwork, and photographs into binary code for computer processing. TurboScan digitizes images at resolutions as high as 300 dpi (dots per inch). Data compression and direct memory access (DMA) transfer of scanned data are supported to reduce scanning time. TurboScan provides two basic scanning modes: line-art mode for black-and-white materials and halftone mode for documents with continuous shading. With 12 built-in screening options for halftones, TurboScan incorporates 14 levels of adjustments for both contrast and brightness. $2,395.
AST Research, Inc., 2121 Alton Avenue, Irvine, CA 92714; 714/863-1333
CIRCLE 317 ON READER SERVICE CARD

A high-speed SMD/SCSI disk controller for the PC/AT and RT PC has been released by **National Memory Systems Corporation**. The **NMS HS8000A** supports disk drives with data rates as high as 2.45MB per second. It is compatible with many networks including those from IBM, Novell, Orchid, 3Com, and Ungermann-Bass. The HS8000A supports the RT under AIX and DOS. It supports the AT under XENIX and DOS, permitting high-speed disk drives of up to 900MB to be formatted up to a single 1,024MB volume. $950.



National Memory Systems' disk controller

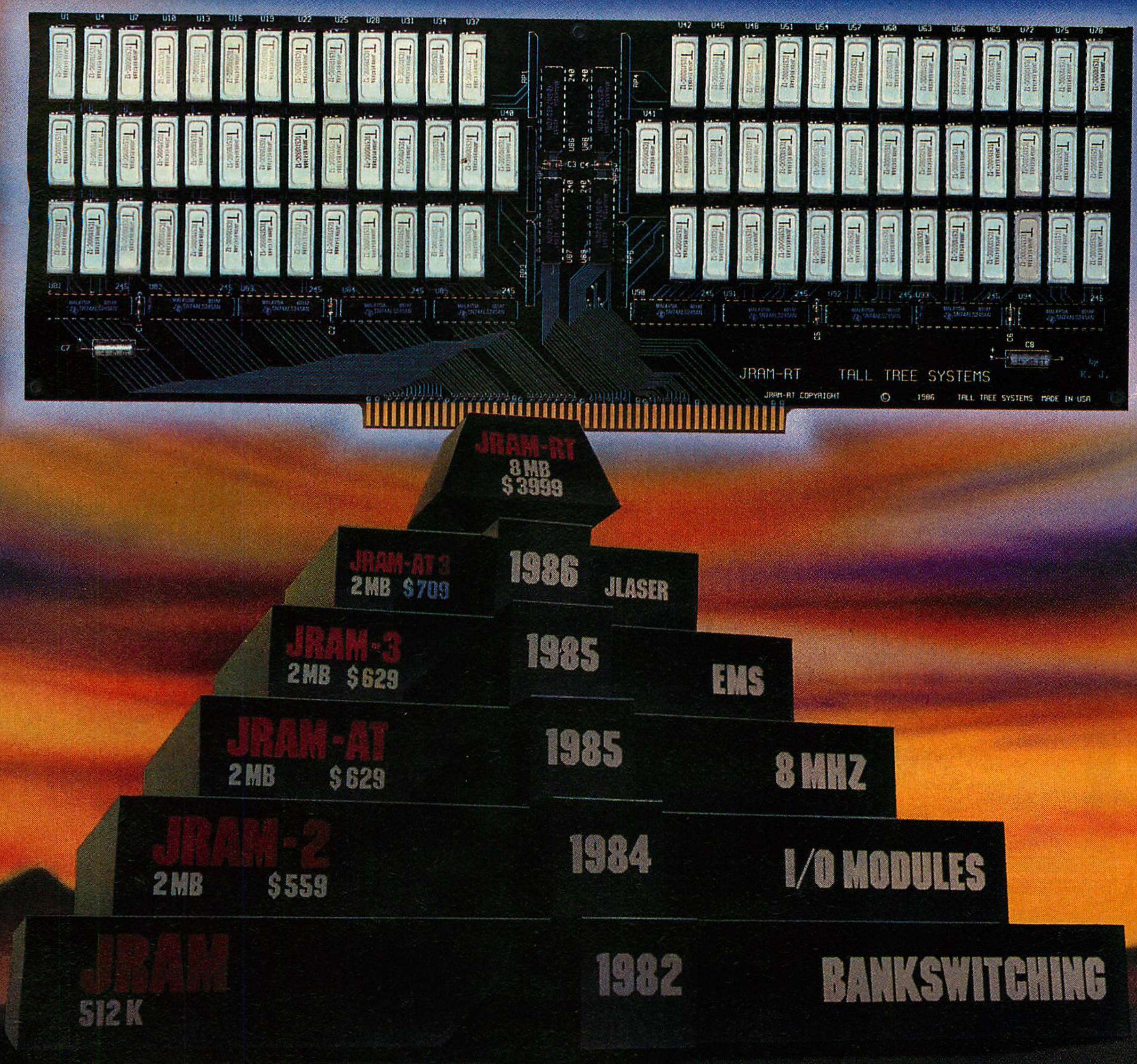
National Memory Systems Corporation, 355 Earhart Way, Livermore, CA 94550; 415/443-1669
CIRCLE 316 ON READER SERVICE CARD

SOFTWARE

XENIX System V/386 and the **XENIX System V/386 Toolkit** have been announced by **Microsoft Corporation**. The Toolkit provides software development tools and an execution environment that will allow software developers to begin creating new XENIX 386 applications before the release of XENIX System V/386 (scheduled for early 1987). All 80386 applications developed using the Toolkit will execute without recompilation under XENIX System/386, and all applications created under the 80286 release will run under XENIX System V/386. XENIX 386 provides access to the large linear address space of the 80386 and a 32-bit data type. The Toolkit includes a Microsoft C compiler for the 80386, a new version of the Microsoft Macro Assembler—extended to support the 80386 instruction set and addressing modes, and a debugger for 80386 programs. Toolkit, $395.

Microsoft also announced the shipment of retail **version 1.03** of its **Windows** operating environment. The new version includes additional device drivers for high-resolution printers and displays, support for AT&T computers, and DOS 3.2 support. Windows 1.03 also supports the Post-Script page description language from Adobe Systems. $99.
Microsoft Corporation, 16011 N.E. 36th Way, P.O. Box 97017, Redmond, WA 98073-9717; 800/426-9400
CIRCLE 324 ON READER SERVICE CARD

The Software Link, Inc. is developing a multiuser operating system for Intel's 80386 microprocessor. **PC-MOS/386** (PC-MultiLink Operating System/386) is a complete native architecture operating system that is fully DOS-compatible. Standard multiuser/multitasking features of PC-MOS/386 include support for record and file locking, intertask communication through the NETBIOS protocol,



TALL TREE SYSTEMS.
A Technological Innovator.
Always a Step Ahead!

For true industry leadership, look no further than Tall Tree Systems.

We have a history of being first.

We were the first to introduce bankswitching. The first with two megabyte memory boards. The first with I/O modularity in a single slot. The first with 8 MHz speed capabilities. The only maker of single command EMS boards. The first with a laser printer solution — JLASER — that allows you to do full-page graphics and multiple type fonts on any Canon® or Ricoh® laser engine.

Now, we're first again with memory expansion for the IBM®RT.

Innovation is our tradition.

Our trademark is superior technology at the lowest possible price.

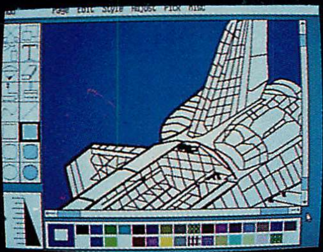
TALL TREE SYSTEMS

1120 San Antonio Road • Palo Alto, CA 94303 • (415) 964-1980

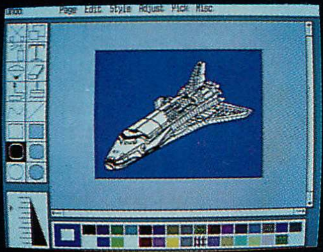
CIRCLE NO. 197 ON READER SERVICE CARD

Unlock your desktop with Publisher's Paintbrush.™

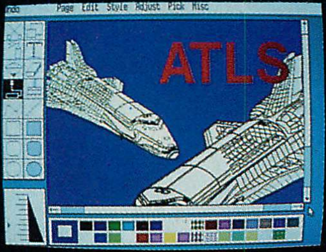
Finally, a paint package designed for desktop publishing! When you create or scan a 300 dpi page, you'll get a 64-screen computer image. That's why Publisher's Paintbrush lets you zoom out and work on the big picture. So you get ultra-sharp resolution without ultra-tedious labor.



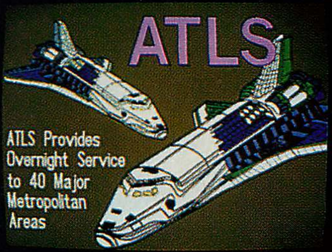
One screen of a 64-screen image.



Shrink down to a manageable size.

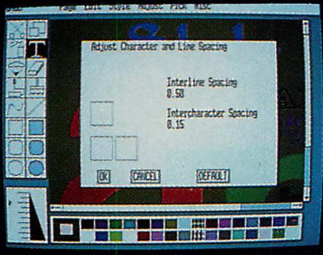


Next, cut-and-paste . . .

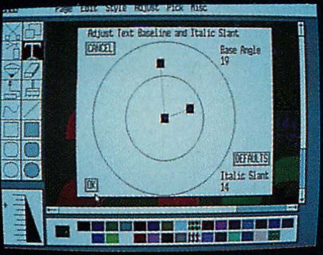


A few edits later . . . VOILA!

New typography frontiers: continuously adjustable point sizes, text slope, line and character spacing, extended and condensed type, and letter slant.

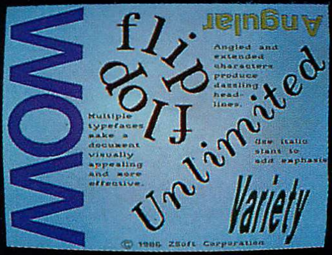


Easy-to-use menus.



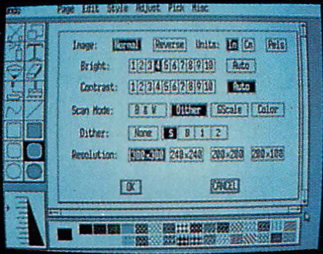
Slant and angle text 1° – 359°.

4- to 250-point type.

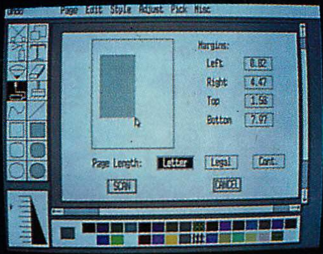


Adjustable everything!

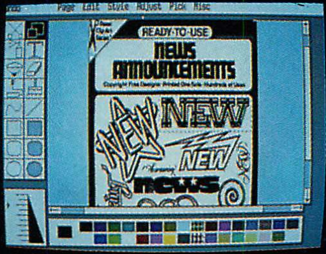
Publisher's Paintbrush adapts to most scanners with absolute simplicity. Scan in existing art, logos and diagrams to save many hours of work!



Full use of scanner features.



Scan all or part of a page.



Combine art and type . . .

. . . from several sources!

Publisher's Paintbrush is a quantum leap in power beyond our top-selling PC Paintbrush®. In fact, it's the dawn of a new era for desktop publishing. With it, you can produce pictures of super-high resolution (many times sharper than your screen!) and marry them into text pages. With it, you can take full advantage of desktop publishing packages, laser printers and image scanners. Without it, you're stuck with ragged edges and tedious multi-screen editing.

Publisher's Paintbrush supports major-brand image scanners and hundreds of printers and video display boards. And most desktop publishing packages have built-in links to Publisher's Paintbrush.

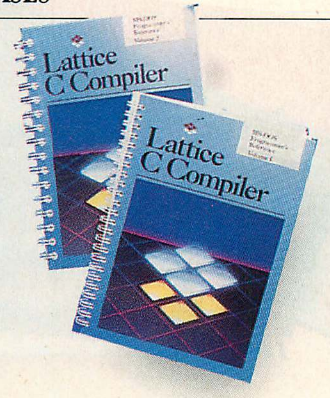
Say goodbye to the old boundaries. Say "Show me" to your ZSOFT dealer. Or call our corporate offices for more information.

Publisher's Paintbrush is a trademark and PC Paintbrush is a registered trademark of ZSoft Corporation. Dover Clip-Art Series is a registered trademark of Dover Publications, Inc.

Z·SOFT

1950 Spectrum Circle, Suite A495, Marietta, Georgia 30067, (404) 980-1950

CIRCLE NO. 184 ON READER SERVICE CARD



Lattice C Compiler version 3.1

PageMaker from Aldus Corporation

print spooling, remote modem access, usage statistics, nested batch files, and security at the user, file, and directory levels. PC-MOS/386 is scheduled for release in February 1987.
The Software Link, Inc., 8601 Dunwoody Place NE, Suite 632, Atlanta, GA 30338; 404/998-0700
CIRCLE 326 ON READER SERVICE CARD

Lattice, Inc. has released **version 3.1** of its **C Compiler**. Case sensitivity with external symbols, enhanced capabilites for generating detailed debugging information, minor fixes to the library and header files are some of the new features. The library contains more than 325 functions compatible with UNIX, XENIX, and ANSI, and has extensive support for DOS versions 2.x and 3.x. Version 3.1 includes a new two-volume *Programmer's Reference Manual*, an object module librarian and disassembler, and a set of libraries. $500.
Lattice, Inc., P.O. Box 3072, Glen Ellyn, IL 60138; 312/858-7950
CIRCLE 335 ON READER SERVICE CARD

SCO XENIX-NET, the version of Microsoft Networks for XENIX, has been announced by **The Santa Cruz Operation**. SCO XENIX-NET is a LAN for computers running XENIX System V; it permits the integration of multiple XENIX systems, or mixed DOS and XENIX systems. SCO XENIX-NET uses an extended file-naming syntax that allows any XENIX application to transparently access any file on any DOS or other XENIX system on the network. SCO XENIX-NET is available for the PC/AT and compatibles using the IBM PC Network interface card and will soon be compatible with EtherNet and Token-Ring. Single-server license format, $595; three-server license format, $1,295.
The Santa Cruz Operation, 400 Encinal Street, Santa Cruz, CA 95060; 408/425-7222
CIRCLE 329 ON READER SERVICE CARD

An assembler/linker for Intel's 80386 microprocessor has been released by **Phar Lap Software, Inc.** The **386/ASM** software package runs on IBM PC, DEC VAX, and other UNIX host computer systems. The 386/ASM is upward compatible with Microsoft 8086 MASM; it supports the same instruction mnemonics, assembler directives, macro language, and expression formats. The 386/ASM also can assemble 8086/286 protected mode programs. PC version, $495; VAX/VMS version, $4,995.
Phar Lap Software, Inc., 60 Aberdeen Avenue, Cambridge, MA 02138; 617/661-1510
CIRCLE 327 ON READER SERVICE CARD

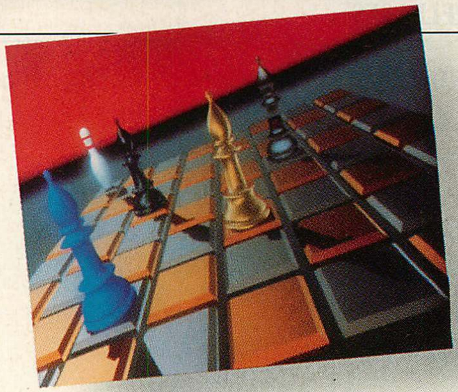
Softguard Systems, Inc. announced it is developing a virtual machine operating system for Intel 80386-based microcomputers. Called **VM/386**, it will allow one 80386-based computer to be several virtual computers. The virtual computers can run concurrently, each with its own operating system. VM/386 also can be used with 80386-based network file servers and 80386 accelerator boards that plug into a PC/AT. VM/386 is modeled after the VM/370 operating system that runs on IBM/370 and 4300 mainframes. Priced under $300.
Softguard System, Inc., 2840 San Tomas Expressway, Suite 201, Santa Clara, CA 95051; 408/970-9240
CIRCLE 328 ON READER SERVICE CARD

Xerox Corporation has introduced **Ventura Publisher Edition**, the first software product from the Xerox Desktop Publishing Series. The package allows the PC to merge text and graphics to create publishing-quality documents. It runs on the PC/XT, PC/AT, Xerox 6065 PC, and supports laser printers such as the Xerox 4045 Laser CP, the Apple LaserWriter, and the Hewlett-Packard LaserJet. It also supports phototypesetters. The interface is such that what the user sees on the screen is exactly what will be printed. Users can enlarge, reduce, or move images within a document; the software will automatically reformat the text around the repositioned or resized image. As text or images are added, the pages are reformatted and numbered automatically. $895.
Xerox Corporation, Xerox Centre, 101 Continental Blvd., El Sequndo, CA 90245; contact the local Xerox dealer; 800/492-4707
CIRCLE 339 ON READER SERVICE CARD

PageMaker, a desktop publishing software package from **Aldus Corporation**, runs on the PC/AT. Under Microsoft Windows, it can directly import preformatted text files created in popular word processing programs; it also can import unformatted ASCII text files and IBM DCA RFT-format (Document Content Architecture Revisable-form Text) files. PageMaker can directly import bitmapped graphics from Microsoft Windows Paint and PC Paintbrush, and Mouse Systems' PC Paint; it imports object-oriented graphics from such programs as Lotus' 1-2-3 and Symphony, and Micrografx Windows Draw! and In*a*Vision. Other types of graphics can be brought into PageMaker through the Windows Clipboard. Documents can be printed on any printer or typesetter supported by Microsoft Windows.

New features include dictionary-based hyphenation for automatic justification, greater control over typographic quality (including kerning), the ability to work with longer publications (up to 128 pages in length and 17 inches by 22 inches in size), the ability to work on facing pages as two-page spreads, multiple type faces and styles, variable type sizes, and line spacing. It has a library of graphic elements, including lines, borders, screens, and patterns. $695.
Aldus Corporation, 411 First Avenue S, Suite 200, Seattle, WA 98104; 206/622-5500
CIRCLE 325 ON READER SERVICE CARD

Network Innovations' Multiplex on Digital's VAXmate



Screen image by Numerical Design's RENDITION

A software accelerator called **PolyBoost** has been introduced by **POLYTRON Corporation**. Without any extra hardware, or modifications of application programs, PolyBoost speeds up the operation of software. PolyBoost is a set of three independent memory-resident programs that speed up the three areas of I/O: disk access, screen display, and keyboard input. A special memory buffer in user RAM, expanded memory, or extended memory reduces the number of times the program has to access a disk or diskette for data. Screen display is accelerated by routing data directly to the screen instead of through DOS or BIOS routines. Keyboard enhancements include a faster repeat rate and a 128-character buffer. $79.95.
POLYTRON Corporation, 1815 N.W. 169th Place, Suite 2110, Beaverton, OR 97006; 503/645-1150
CIRCLE 331 ON READER SERVICE CARD

Informix Software, Inc. (formerly Relational Database Systems, Inc.) has announced enhanced versions of **INFORMIX-SQL**, **INFORMIX-ESQL/C**, and **C-ISAM**, the first available database management software packages based on SQL (structured query language) for DOS-based LANs. The packages are available for licensing in configurations ranging from 4- to 32-node networks and support the IBM Token-Ring Network, IBM PC Net, AT&T STARLAN, Novell Advanced NetWare, 3Com 3Plus, and Ungermann-Bass NET/ONE. INFORMIX-SQL 4-node system, $1,995; up to 32-node system, $14,000; INFORMIX-ESQL/C for 4-node system, $1,495; up to 32-node system, $10,500; C-ISAM for a 4-node system, $450.
Informix Software, Inc., 4100 Bohannon Drive, Menlo Park, CA 94025; 415/322-4100
CIRCLE 332 ON READER SERVICE CARD

TSCOB is a full level-2, FIPS (Federal Information Processing Standard) high-level COBOL compiler from **Taneco Systems, Inc.** Conforming to the highest level of ANSI 1985 and 1974 standards, TSCOB covers all modules plus two extended features: symbolic debugging and screen handling. Also included is an indexed file-management system called **TSIAM** that creates and maintains indexed files on disk or diskette. TSCOB-85, TSCOB-74, and TSIAM, $145: after December 31, 1986, $295.
Taneco Systems, Inc., 17461 Irvine Blvd., Suite K, Tustin, CA 92680; 714/832-3922
CIRCLE 336 ON READER SERVICE CARD

From **Larson Computing** comes an expanded memory simulator for the PC/AT. **LIMSIM** is a software driver that supports ordinary extended memory according to the LIM EMS. Aimed at the AT user who has an add-on memory board that does not support EMS, LIMSIM provides the required interface. LIMSIM also manages the memory on multiple boards. $50; with source code, $75.
Larson Computing, 1556 Halford Avenue, Suite 142, Santa Clara, CA 95051; 408/737-0627
CIRCLE 334 ON READER SERVICE CARD

A compiler for DBASE III PLUS, **Quicksilver**, has been announced by **WordTech Systems, Inc.** Quicksilver offers full support for the programming commands and functions of DBASE III PLUS. Features include memo fields, a superset of Ashton-Tate's networking commands, and fully compatible data and index files. Users have access to enhancements such as user-defined functions, windowing, the ability to link compiled C language routines into DBASE applications, support for DBASE Tools for C, and a maximum of 4,000 memory variables. Compiled code does not need DBASE III PLUS and may be distributed without license fees. $599.
WordTech Systems, Inc., P.O. Box 1747, Orinda, CA 94563; 415/254-0900
CIRCLE 338 ON READER SERVICE CARD

Network Innovations Corporation has announced a version of its **Multiplex** networking package that provides the first link between PC applications and applications for Digital Equipment Corporation's VAXmate databases and data files on VAX minicomputers (see the HARDWARE section). Multiplex automatically handles all database inquiry, data reformatting and data communications tasks. Multiplex has a Lotus-style user interface and a Lotus-style macro facility. Multiplex can bring selected data across the network from the VAX host into a VAXmate file and automatically reformat it into standard PC formats. PC configuration, $695.
Network Innovations Corporation, 20863 Stevens Creek Blvd., Cupertino, CA 95014; 408/257-6800
CIRCLE 333 ON READER SERVICE CARD

RENDITION, an ultra-high-quality rendering software package developed by **Numerical Design, Ltd.** has been enhanced with several features. RENDITION consists of a set of programs that generate high-quality images from polygonal object and appearance data that is supplied by the user; transparent objects are supported in this enhanced version. The texture mapping feature permits mapping a two-dimensional image onto the surface of an object in three-dimensional space. RENDITION is compatible with the LIM EMS, enabling users to produce complex images more easily. The addition of a shadow-generation feature enhances the three-dimensional feel of an illustrated scene. Package available in OEM quantities, $2500.
Numerical Design, Ltd., 133 E. Franklin Street, P.O. Box 1316, Chapel Hill, NC 27514; 919/929-2917
CIRCLE 340 ON READER SERVICE CARD

The material that appears in Tech Releases is based on vendor-supplied information. These products have not been reviewed by the PC Tech Journal *editorial staff.*

Over 5 Years.
More Than 2,000,000 Times.
AST Has Increased
The Power Of The PC.
Now, Out Of This Experience
Emerges A Powerful And
Versatile Personal Computer.
Built On Proven Technology.
Enhanced Like No Other.

Announcing
AST Premium/286.™

Discover AST Premium/286. The First
AST Quality, Uncompromising AT® C

More than two million people have made us the first choice in PC Enhancement. For over five years, you've known AST as the leading PC enhancement company. Now, we're introducing the ultimate enhancement: AST Premium/286. The first AT-compatible personal computer with AST performance and reliability. More flexible and upgradeable. Skillfully combining lightning fast processing speed and uncompromising compatibility.

AST FASTslots:™ Processing speedways. Forming the foundation of the AST Premium/286's increased speed are our FASTslots. This advanced architecture improves overall performance so there's enough built-in power to satisfy even the most demanding user.

The AST Premium/286 operates 50% faster than an 8MHz PC AT® as measured by the Norton Utilities™ Version 3.0 SysInfo. And maintains full compatibility with standard PC and AT-based enhancement cards. It also provides for a powerful, easily upgradeable and expandable future, accommodating the next generation of accelerator and high-performance enhancement cards.

A Heritage Of Software Compatibility. Software compatibility has always been one of our strong points. Shipped with the industry-standard MS-DOS® 3.1, AST Premium/286 is compatible with widely accepted operating systems such as IBM® PC-DOS,™ Concurrent DOS™ and XENIX.™ It's also designed to get the most out of multitasking software packages like Microsoft® Windows, DESQview™ and TopView.™

Applications-oriented. Keyboard-selectable operation at 10, 8 or 6MHz means virtually all popular off-the-shelf IBM PC and PC AT application software is immediately compatible. All your favorites, including Microsoft Word, Lotus® 1-2-3,® Framework,™ Symphony,® dBASE® III and AutoCAD.™

Attain your fullest software potential. AST's advanced architecture also provides faster and more flexible memory addressing. While built-in Enhanced expanded memory capabilities—AST FASTRAM,™ expandable to 2MB in a single slot—let you break the 640K DOS barrier. Create bigger spreadsheets and sort larger databases. And enjoy the uninterrupted workflow benefits of multitasking using current DOS versions, with full support for protected mode software built-in.

Fast access disk storage. Complementing AST Premium/286's speedy operation is a full line of disk systems. There's a 20MB, 40MB and a 70MB hard disk. Both the 40MB and the 70MB offer more storage and faster access times—below 30msec—than the PC AT's fixed disk. And our external disk/tape systems, featuring advanced SCSI architecture, allow easy expandability.

Prices Start At $1995.00*

Personal Computer With Legendary ompatibility and Lightning Speed.

More standards are standard. We build-in our AST FASTRAM™ memory card. And most models include our own multi-mode enhanced graphics adapter, supporting IBM EGA, CGA and Monochrome, and Hercules Graphics Card™ display modes.

Compatible with AST and IBM Products. AST Premium/286 is designed to remain your productivity partner for years to come. Choose it with confidence for single and multitasking applications, individual and shared environments alike. Use it as an engine with other AST products to form powerful application workstations for desktop publishing, CAD/CAE and more. Or to increase connectivity use it as a network file server, to communicate with IBM mainframes and minicomputers, or to manage multiuser environments.

Solutions that are ready to go. We also offer a number of pre-configured workstation solutions tailored for maximum performance in your application. Combining our proven products, from local area networking and data communications to extra memory and I/O to laser printers and disk systems, our solutions are all designed to increase your business productivity.

Quality across the board, around the world. When you buy AST products, you're also purchasing a worldwide reputation for service, support and product dependability. AST Premium/286 is backed by a one year limited warranty, and our worldwide network of certified dealers and service centers.

AST Premium/286—The system and the solutions. For more information call our Product Information Center at **(714) 863-0181** or send the coupon to: AST Research, Inc., 2121 Alton Avenue, Irvine, CA 92714-4992.

Yes, I want to know more about AST Premium/286 Solutions. Send me more information today.

Name:__________

Title:__________

Company:__________

Address:__________

City:__________ State:__________

Zip:______ Telephone:(____)______

My applications:

____ Desktop Publishing ____ Multiuser
____ Mainframe/Minicomputer Connection
____ Multitasking ____ General Business

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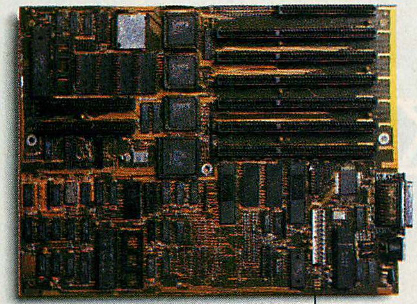
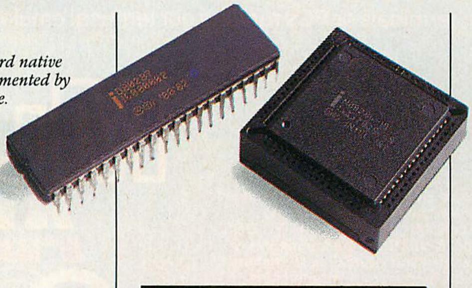
AST Research, Inc., 2121 Alton Avenue, Irvine, CA 92714-4992 Attn: M.C. PCTJ 12/86
01PCTH000B01PM

AST RESEARCH INC.

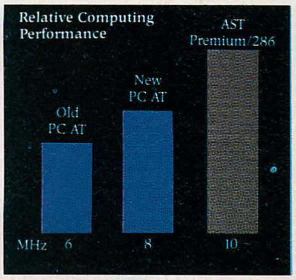


Seven industry-standard expansion slots; 1 PC-compatible slot, 6 PC AT-compatible slots, including two AST FASTslots. FASTslots provide no wait state operation with a high-speed direct interface to the 10MHz 80286 processor. Advanced architecture accommodates the next generation of accelerator and high-performance enhancement cards. It's also an open architecture for easy development and system integration.

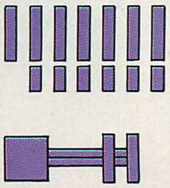
Based on industry-standard native 80286 technology, complemented by AST advanced architecture.

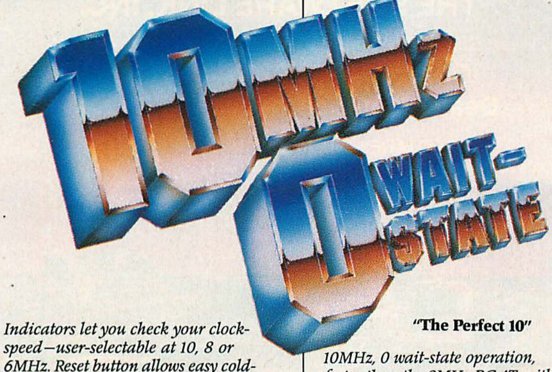


Coprocessor socket accepts 8MHz 80287 devices to execute math- and floating point-intensive programs faster.



Compare the increased speed of the AST Premium/286 against the top competitors for yourself. (Basis: Norton Utilities SysInfo Version 3.0)



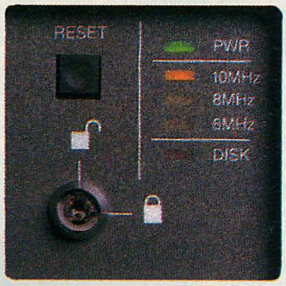


Two AT-compatible expansion slots with a plus: a third bus connector featuring lightning-quick CPU access time, for use with specially-designed cards like the AST FASTRAM Enhanced memory card. Expandable to 2MB in single slot, FASTRAM supports a variety of addressing capabilities—Enhanced EMS, EMS, extended (protected mode) and conventional memory addressing.

Enhanced, low-profile 101/102-key keyboard with separate numeric keypad, dedicated cursor control and extra function keys. International versions available.

AST Premium/286 is shipped with MS-DOS and GW BASIC® and it's fully compatible with a wide variety of operating systems, operating environment and utility packages, and application software.

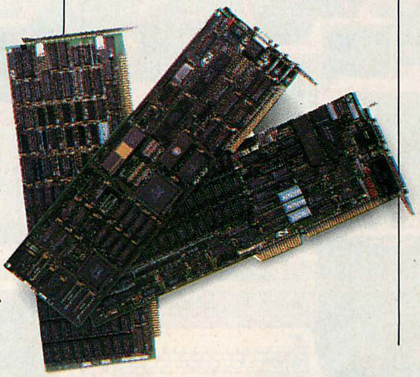
Indicators let you check your clock-speed—user-selectable at 10, 8 or 6MHz. Reset button allows easy cold-booting. Security lock prevents unauthorized keyboard access.



"The Perfect 10"

10MHz, 0 wait-state operation, faster than the 8MHz PC AT, with IBM PC AT hardware and software compatibility.

Supports standard PC, PC AT and AST FASTslot cards. With AST, you start with a lot, like our included FASTRAM Enhanced memory card and multimode Enhanced Graphics Adapter, but you've also got a lot of options. We offer the widest range of compatible enhancement products and peripherals to suit your needs—a true one-stop solution allowing you to expand and upgrade your system with the assurance of future service and support.



AST markets products worldwide—in Europe call: 44 1 568 4350; in the Far East call: 852 0499 9113; in Canada call: (416) 826-7514.

To Over 30,000 Installations, MultiLink® MEANS Multi-User.

At over 30,000 sites, as many as one-quarter of a million users tap into the power of MultiLink® Advanced everyday.

Since 1983, they've come to rely on our multi-tasking, multi-user system for compatibility with their favorite software, and the ability to share disks, files, printers, and programs in a *true* PC-DOS environment.

From the largest of the Fortune 500 to the smallest in small business, MultiLink® has provided a cost-effective multi-user solution that's available from no one else.

MultiLink® Means Cost-Effective Timesharing on a PC. MultiLink® Advanced utilizes the principle of timesharing by sharing a central PC's peripherals, files, and processor time among nine users. Up to eight inexpensive terminals can be connected to a single non-dedicated IBM PC, XT, AT or 100% compatible using standard RS-232 ports. Each terminal effectively emulates a PC having up to 512K RAM.

PC-Shadow™ Workstations, shown below, even have an AT look-alike, as well as work-alike, keyboard, display, and serial port. In addition, password-protected remote access via modem can be made with either dumb terminals or PCs running our terminal emulation software.

MultiLink® Means PC-DOS Compatibility with a *Software-Driven* System. Lotus 1-2-3, Symphony, WordStar, dBASE III, & Multimate are just a sampling of the wide variety of PC-DOS software that's fully compatible.

Our software-driven system is also IBM NETBIOS compatible, so programs that are written for IBM's Token Ring will run on our multi-user system, as well.

MultiLink® Means Multi-User to Leading Computer Publications. Whether you read *PC Magazine*, "MultiLink® Advanced delivers on...convenience, speed, and flexibility," or *InfoWorld*, "If you want a low-cost multiuser system with up to eight terminals, MultiLink® Advanced is worth a serious look," it becomes clear that MultiLink® Advanced is a formidable contender in the multi-user marketplace.

See What MultiLink® Can Mean to You. Learn, firsthand, how our multi-user system can benefit your company. Call The Software Link TODAY for complete information and the authorized dealer nearest you. MultiLink® Advanced is $595 and comes with a money-back guarantee.

MultiLink®
ADVANCED

THE SOFTWARE LINK, INC.

8601 Dunwoody Place, Suite 632, Atlanta, GA 30338 Telex 4996147 SWLINK

CALL: 404/998-0700

Dealer Inquiries Invited

THE SOFTWARE LINK, INC./CANADA
250 Cochrane Drive, Suite 12 Markham, Ontario L3R 6B7
CALL: 416/477-5480

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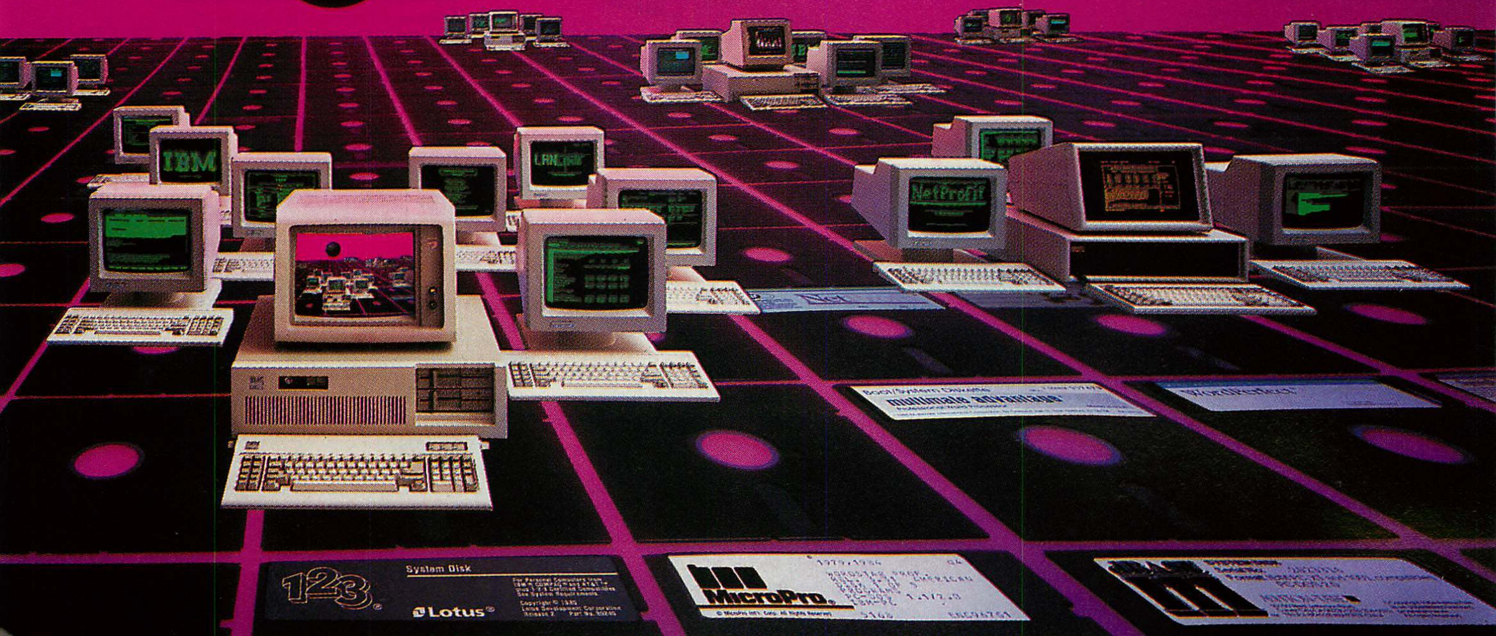

In celebration of the season...

We'd like to wish everyone a warm Season's Greetings and thank our customers for their valued support.

We're celebrating the holiday season by offering some great products at fantastic savings through the end of this year – our holiday gift to you.

As a Programmer's Connection customer, you'll be treated to the finest service possible. We understand the importance of the personal touch and we'll make your buying experience a pleasant and rewarding one.

It's our dedication to quality service and low prices that sets us apart from the other dealers in this industry. So make the connection today and discover the difference for yourself. You'll be glad you did.

Please refer to our product list on the next two pages for price information.

Buy any supported C, FORTRAN or Pascal compiler at our regular price and get **MetaWINDOWS** or **MetaWINDOWS/Plus** by MetaGraphics for **50% off** the retail price.

Buy **Turbo PASCAL** at our regular price of **$65** and get **MetaWINDOWS** or **TurboWINDOW** by MetaGraphics for **50% off** the retail price.

Buy **Microsoft FORTRAN** or **RM/FORTRAN** at our regular price and get any **Alpha Computer Service product(s)** for **50% off** the retail price.

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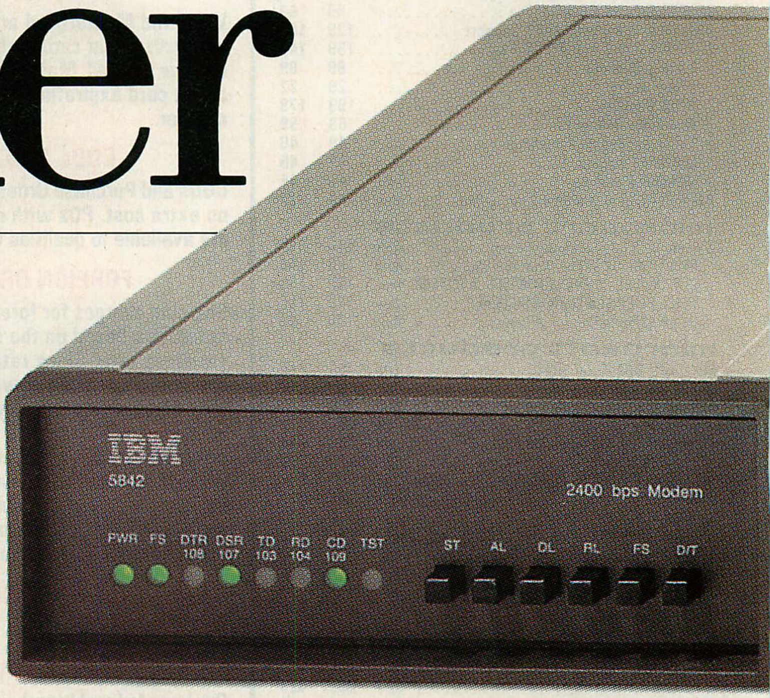

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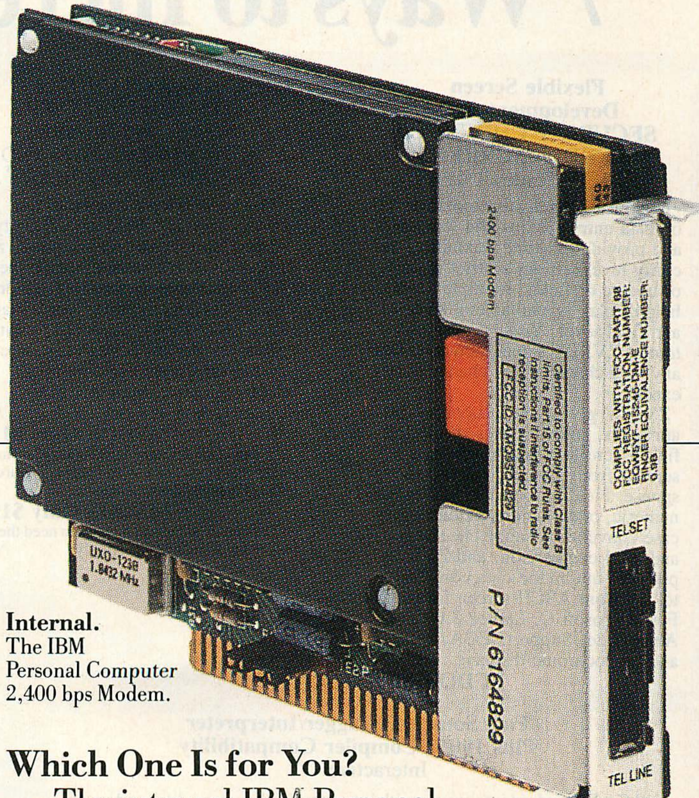

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TECH NOTEBOOK 70

WILLIAM F. POLIK

Large Turbo Pascal Arrays

Using the heap, Turbo Pascal can overcome its 64KB limitation in implementing two-dimensional arrays.

Although Borland's Turbo Pascal is recognized as being one of the most versatile languages for the IBM PC, its major limitation is that it produces .COM files with data segments no larger than 64KB. One standard way of increasing data space is to use the *heap*, which is free memory between the top of the declared data space and the bottom of the stack (and can easily be as large as 400KB on a 640KB system). Data are dynamically allocated onto the heap with the standard procedure **new** and are accessed with pointers, which in Turbo Pascal are addresses pointing to variables on the heap. Using the heap dramatically increases the amount of data space available to a Turbo Pascal program because each pointer requires only four bytes in the data segment to point to a variable that may be as large as 64KB.

Many standard calculations, such as solving a system of linear equations, performing a statistical analysis on a data set, or determining eigenvectors and eigenvalues, are best formulated using two-dimensional arrays. A 64KB data segment limits the size of such matrices to 90-by-90 for 8-byte Turbo-87 Reals, assuming no other variables are required. Using a 400KB heap for data storage would allow the creation of a 223-by-223 matrix without exhausting the 64KB of the data segment available for storing all other variables.

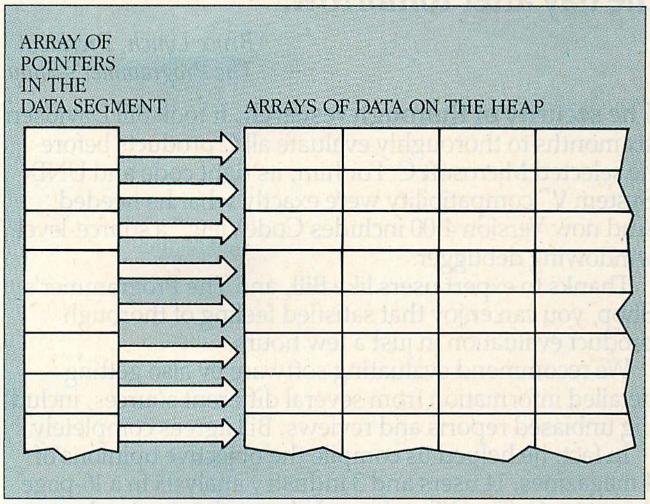
The trick to using the heap for storing a two-dimensional array is to create a one-dimensional array of pointers, each of which points to a row of the matrix (figure 1). Each element of the array is referenced by its row pointer and its column position—that is, A[row,column] becomes A[row]^[column]. The similarity in expression of a static array element to a heap array element results in very readable source code and allows easy recoding of existing routines for larger matrices.

The code implementation of a large two-dimensional array is illustrated in figure 2. The type RowArray is declared to represent each row of the matrix. The variable *A* is an array of pointers, each pointing to a RowArray. Before any array element can be accessed, space must be allocated on the heap at runtime for the matrix. This is conveniently done with a FOR loop. Note that the array elements are not initialized (neither are the usual static array elements declared in the data segment). Array elements stored on the heap may be used in any place where static array elements are allowed.

Using the heap to store arrays allows for the creation of matrices that are limited only by the amount of memory in the computer. The resulting Turbo Pascal code remains quite readable, and existing applications can be easily recoded to handle larger arrays.

William F. Polik is a National Science Foundation predoctoral fellow in the department of Chemistry, University of California, Berkeley. His interests include the use of computers for education in chemistry.

FIGURE 1: *A Matrix on the Heap*



Each pointer points to a one-dimensional array of real numbers, which results in a two-dimensional matrix.

FIGURE 2: *Pascal Implementation*

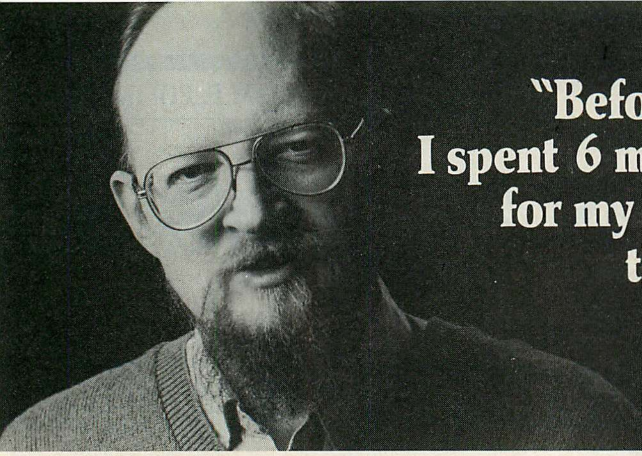
```
CONST
  MaxCols = 200;               { For a 200x200 matrix }
  MaxRows = 200;

TYPE
  RowArray = Array[1..MaxCols] of Real;

VAR
  A : ARRAY[1..MaxRows] of ^RowArray;
  i : Integer;

BEGIN
..
..
FOR i := 1 TO MaxRows DO   { Must allocate space on heap! }
  New(A[i]);
..
..
A[113]^[42] := 5.38;          { Use matrix elements as usual }
A[75]^[187] := 10.76/A[113]^[42];
WriteLn(A[75]^[187]);
..
..
END.
```

This fragment of a Turbo Pascal program implements a 200-by-200 matrix of real numbers on the heap.



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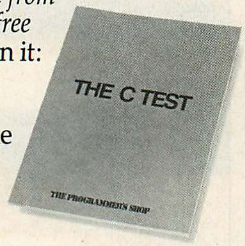

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ARSEN DARNAY

Reading Locked Files

Two routines allow the user to overcome a Turbo Pascal bug and read locked files.

To lock a file as read-only under DOS, the DOS ATTRIB command can be used:

C>attrib +r myfile.txt

Using -r would unlock the file and using ATTRIB alone would display the attribute of the file on screen.

In Turbo Pascal, a serious bug in the compiled code prevents *reading* of locked files as well as writing to them. Attempting to open a locked file generates I/O Error 01, "File does not exist," even though it does exist.

ROREADER.PAS provides two routines to unlock files and restore the write protection after reading them. DOS function 43H (change file mode) can obtain or set the current attribute. The call is made with AH holding 43H and DS:DX pointing to an ASCII path name terminated by 0H. To *read* the attribute, set AL to 0H, and CX returns the attribute byte. To *write* the attribute, set AL to 1H; CX must hold the desired attribute. For both, the carry flag will be set on error (no file found). AX holds the error code.

Clear_Attribute reads and changes the attribute from within Turbo Pascal. The low bit of the attribute byte, obtained with function call 43H and placed into CX, controls read only status. If the bit is 1, then the file is locked. Clear_Attribute also checks the attribute; if the file is unlocked, it returns after saving the attribute. If the file is locked, the attribute is changed by clearing its low bit and writing it back again. This routine is called before opening the file to avoid an error on trying to open a locked file.

Restore_Attribute is called after file close, restoring the attribute, so that a file that was locked on entry is locked on exit. Clear_Attribute and Restore_Attribute are for *reading* files and should not be used for writing to a file.

Arsen Darnay is a computer consultant and author.

LISTING: ROREADER.PAS

```
PROGRAM ROReader;

Type Regpack = Record Case Integer of
               1:  (AX,BX,CX,DX,BP,SI,DI,DS,ES,FLAGS:  Integer);
               2:  (AL,AH,BL,BH,CL,CH,DL,DH          :  Byte);
               End;
String40 = String[40];

Var Target:   Text;
    Fname:    String40;
    F_Attr:   Integer;
    Myfault:  Integer;
    Regs:     Regpack;
    Textline: String40;

{This procedure checks the attribute of a file.  If file is write-
protected, it saves the current attribute of the file and unlocks it.}
procedure clear_attr(Fname : String40);
Var TempName: String40;
BEGIN
     TempName := Fname + Chr(0);         {User's pathname in Fname}
     WITH Regs DO                        {  Cap with 0H for DOS   }
        Begin
          AL := $00; AH := $43;  DS := Seg(TempName);
          DX     := Ofs(TempName) + 1;   {Go 1 beyond Length byte}
          F_Attr := 0;                   {Clear our attribute}
          CX     := 0;                   {Clear CX for good measure}
          MsDOS(Regs);
         If (Flags AND $1 <> 0) then Exit;
         F_Attr := CX;                   {Save attribute}
         If Odd(CX) then                 {If locked CX will be odd}
             Begin
               AL := $01;                {Set for writing}
               AH := $43;
               CX := CX AND $FE;         {Turn off low bit}
               DS := Seg(TempName); DX := Ofs(TempName)+1;
              MsDOS(Regs);
             End;
        End;
END;

{ This procedure restores a file attribute.  The attribute is stored
in F_Attrib.  The user has stored the file name in variable Fname.}
procedure restore_attr(Fname : String40);
Var TempName: String40;
BEGIN
     TempName := Fname + Chr(0);         {Cap name with 0 for DOS}
     With Regs Do
        Begin
          AL := $01;                     {Set write mode}
          AH := $43;
          DS  := Seg(TempName); DX  := Ofs(TempName) + 1;
          CX  := F_Attr;                 {Write old attribute out}
          MsDOS(Regs);
        End;
     F_Attr := 0;                        {Clear our attribute var}
END;
BEGIN
     Fname := 'LOCKTEST.TXT'; Assign(Target,Fname);
     Clear_Attr(Fname);
     {$I-}  Reset(Target)  {$I+};
     MyFault := IOResult; If MyFault <> 0 then
        Begin
          Writeln('Error #',MyFault,' on file open.');
          Exit;
        End;
     While NOT EOF(Target) DO
       BEGIN
         Readln(Target,Textline);
         Writeln(Textline)
       END;
     {$I-}  Close(Target)  {$I+};
     MyFault := IOResult;
     If MyFault <> 0 then Writeln('Error on file close');
     Restore_Attr(Fname);
END.
```

Before you consider the new Hercules Graphics Card Plus, consider the technology behind it.

A short while ago, Hercules™ introduced a product that will forever change the way information is displayed on a PC.

The product is called the Hercules Graphics Card Plus.

We gave it that name because it gives you the same hi-resolution text and 720x348 graphics that made the original Hercules Graphics Card famous.

Plus it gives you RamFont™.

RamFont is a radical new hardware mode that combines the speed of text mode with the flexibility of graphics mode.

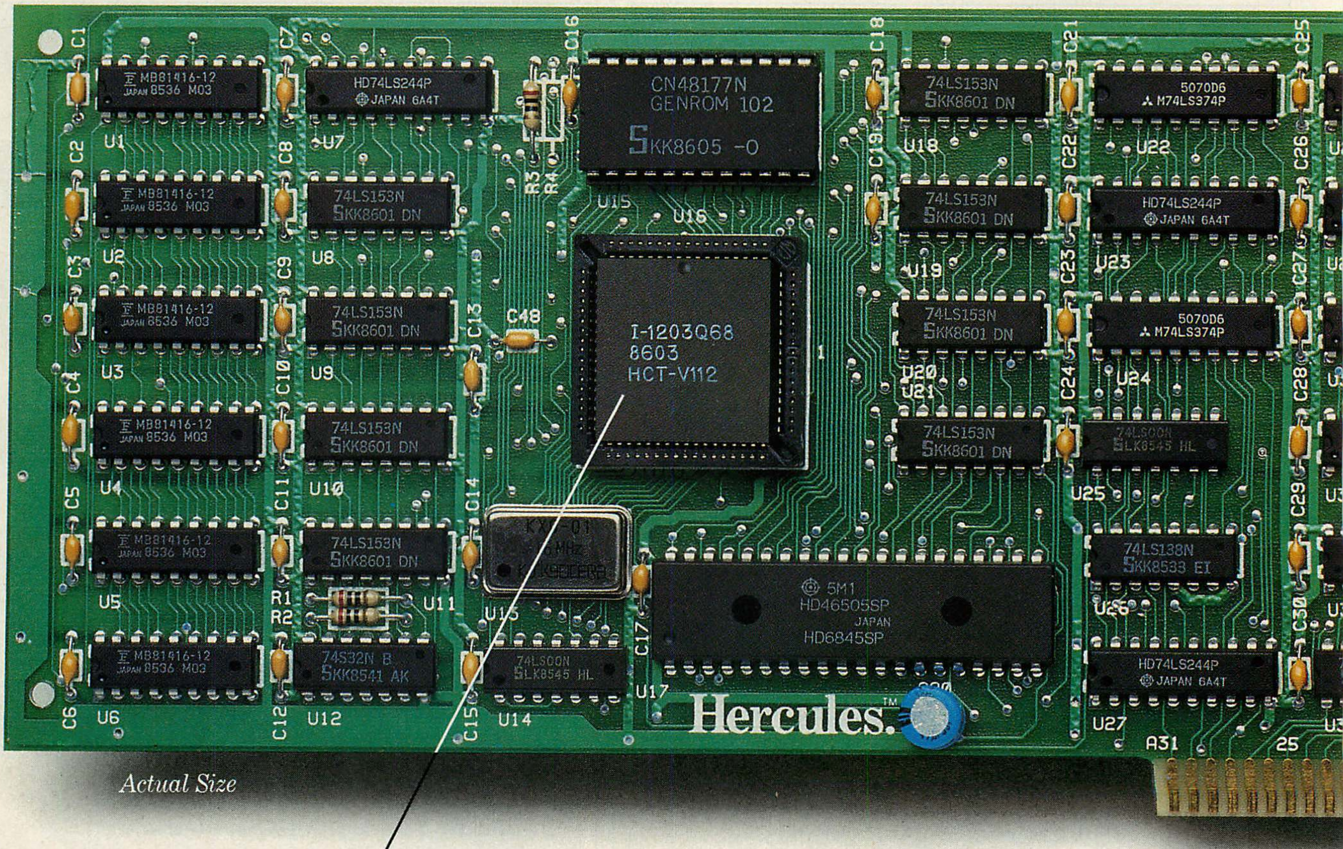
And opens up a whole new world for software.

The world according to RamFont.

In the old days (before the Graphics Card Plus), programs like Lotus® 1-2-3®, Symphony™, Framework™ and Microsoft® Word had to use graphics mode to display multiple fonts and variable text sizes, or to mix text with graphics.

But graphics mode is a whole lot slower than text mode. Up to eight times slower.

Enter RamFont.



Actual Size

The heart of the Graphics Card Plus: the V112 microchip, Hercules' next generation video processor that makes the RamFont mode possible.

It lets all the programs we just mentioned (and plenty more in the future) do all the things we just described, all on one screen.

At precisely the same speed as text mode.

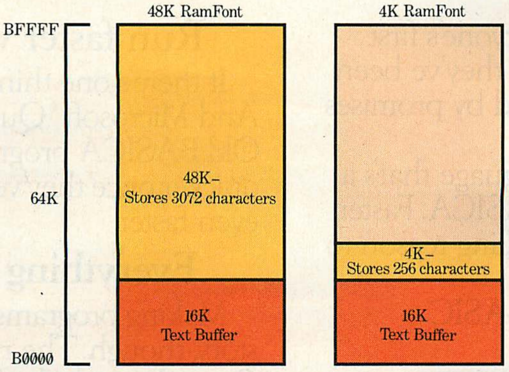
How RamFont works.

Like text mode, RamFont uses a 16-bit word to represent a character on the display.

Unlike text mode, however, the 48K RamFont mode uses a 12-bit character code instead of an 8-bit code.

Which allows you to choose from an astonishing 3072 different characters.

While setting the size of your screen cells from eight to nine pixels wide and from four to 16 scan lines tall.



The new RamFont mode displays 3072 programmable characters at the speed of text mode, or replaces the standard character set with one of your choice in 4K RamFont mode.

To help you design your own RamFont characters and symbols, we've included a font editor called FontMan.™

Along with a set of 25 sample fonts to start your library.

And since the 4K RamFont mode can accept 8-bit character codes, running your text mode software with your favorite font is as simple as loading it into RAM.

Just for the record, RamFont supports the standard character attributes of reverse, high-intensity, blink and underline.

Plus two new RamFont attributes: boldface and strike-through.

What price success?

While we're on the subject of technological breakthroughs, let's not forget the suggested retail price.

$299.
Suggested retail price.

Think of it. You get everything the original card gave you.

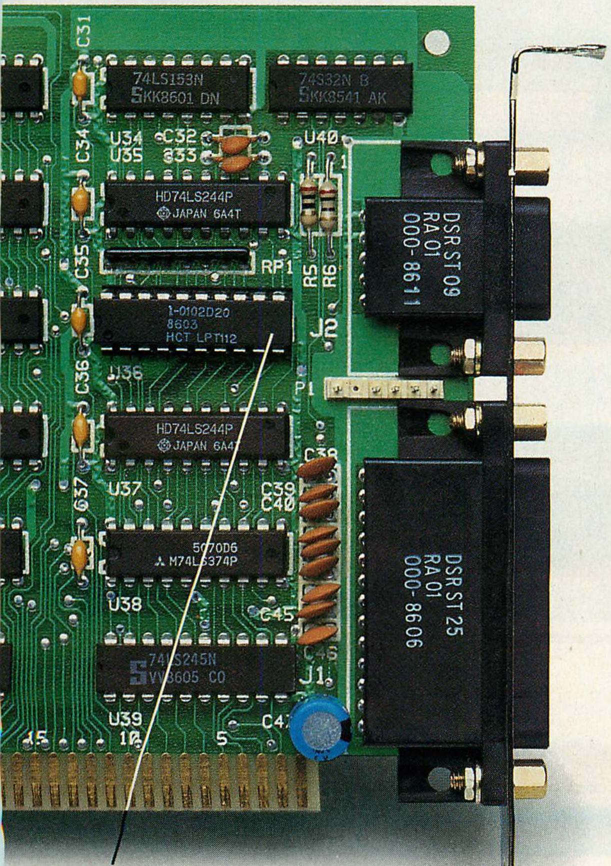
Plus RamFont.

Plus FontMan.

Plus a parallel printer port that you can now disable if there's a conflict with another port in your system.

All for just $299—about half the price of the original Graphics Card.

If you haven't gone into shock, call 1-800-532-0600 ext. 211 (in Canada call 1-800-323-0601 ext. 211) for the name of an Authorized Hercules Dealer near you and we'll rush you our free info kit.



Another Hercules innovation: the new LPT112. It's a parallel printer port on a chip.

Hercules.™

We're strong on graphics.

Address: 2550 Ninth Street, Berkeley, California 94710 Ph: 415 540-6000
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Trademarks/Owners: Lotus, 1-2-3, Symphony/Lotus; Framework/Ashton-Tate; Microsoft/Microsoft; Hercules, RamFont, FontMan/Hercules

CIRCLE NO. 242 ON READER SERVICE CARD

Finally, a language worth

For years BASIC has been everyone's first language. And for almost as long, they've been tempted by other languages. Lured by promises of more speed, more power.

We have a solution. A new language that's a substantial improvement over BASICA. Faster. More structured. Finally, a compelling reason to leave BASIC.

Introducing Microsoft's QuickBASIC Compiler, Version 2.0.

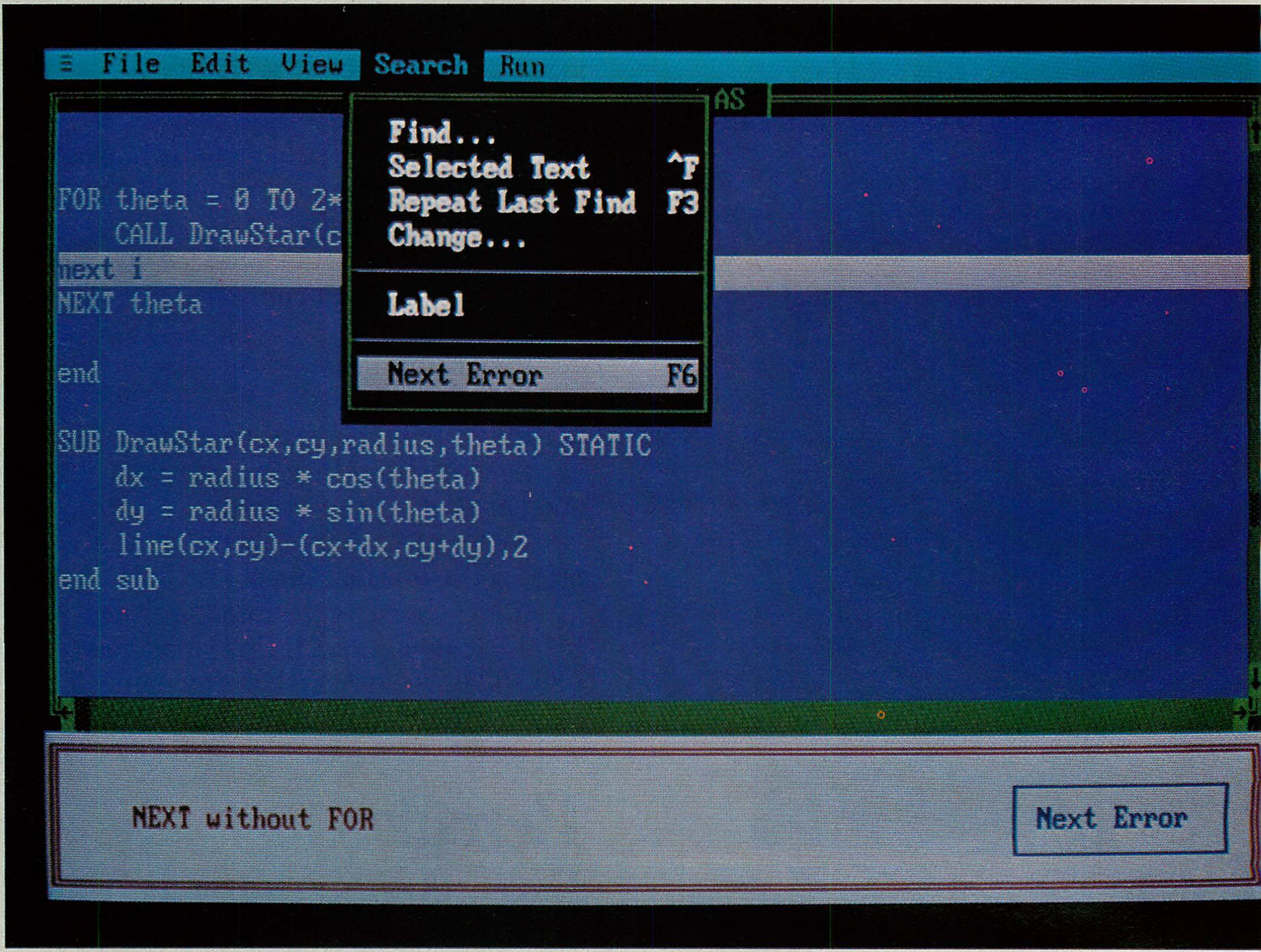
At last, you can have the latest programming techniques, combined with the solid foundation of BASIC. Our new compiler is as compatible with BASICA as you can get. At the same time it offers the extra speed and power you've been looking for.

Run faster with compiled code.

If there's one thing you've asked for, it's speed. And Microsoft® QuickBASIC simply blazes. Old BASICA programs will run up to ten times quicker once they've been compiled. Sometimes even faster.

Everything you need. Built-in.

Making programs run faster is only part of the story, though. The new Microsoft QuickBASIC Compiler includes a full-screen editor, built-in. So now you can make the jump from writing to RUNning in no time flat. Edit your program, compile it, and run it. Faster than any other BASIC compiler around. All without leaving our on-line help and prompts.



leaving BASIC for.

On the rare chance your program doesn't run 100% the first time out, we've got another surprise for you. The Microsoft QuickBASIC debugger. Our full-screen tracing lets you debug your programs while watching the source code execute. A line at a time, or with breakpoints. As easy as can be.

Our compiler is also smart enough to save you time. First, by finding any errors in one pass. Second, by putting your editor's cursor on the problem. Automatically. So you don't have to get lost in a maze of error codes and line-numbers.

The BASIC virtues. And more.

Speaking of line numbers, let's not. Because line numbers are strictly optional. And Microsoft QuickBASIC lets you use alphanumeric labels as well. Now you can GOTO *ErrorCheck* instead of line number 6815.

Or you could stop using GOTOs altogether. There are a variety of options that could make the GOTO an endangered species. Features like multi-line IF-THEN blocks. And named subprograms. Now your BASIC programs can be as structured and organized as you want.

We've only just begun to talk about the virtues of Microsoft QuickBASIC. There are dozens of enhancements to your favorite language. Things like larger arrays. Local and global variables. Reusable modules that let you create libraries of your most often-used routines. All explained in a revised manual that includes a complete language reference.

Making your quick escape.

If all these features follow your BASIC instincts, then zip on down to your nearest Microsoft dealer. That's where you'll discover the best surprise of all. The price. Only $99 for the best reason to leave BASIC.

For the name of your nearest Microsoft dealer, call (800) 426-9400. In Washington State and Alaska, (206) 882-8088. In Canada, call (416) 673-7638.

Microsoft® QuickBASIC
The High Performance Software™

Microsoft QuickBASIC Compiler Version 2.0 for IBM® PC and Compatible Computers.

BASICA Compatibility
- Sound statements including SOUND and PLAY.
- Graphics statements including WINDOW, VIEW, DRAW, GET, PUT, LINE, CIRCLE, LOCATE and SCREEN.
- Support of EGA extended graphics modes. NEW!
- BASICA structures are supported including WHILE/WEND, IF/THEN/ELSE, FOR/NEXT, GOSUB/RETURN, and event handling.

Results of Sieve Benchmark	BASICA 3.1	Microsoft QuickBASIC 2.0
Seconds per iteration	78	0.52

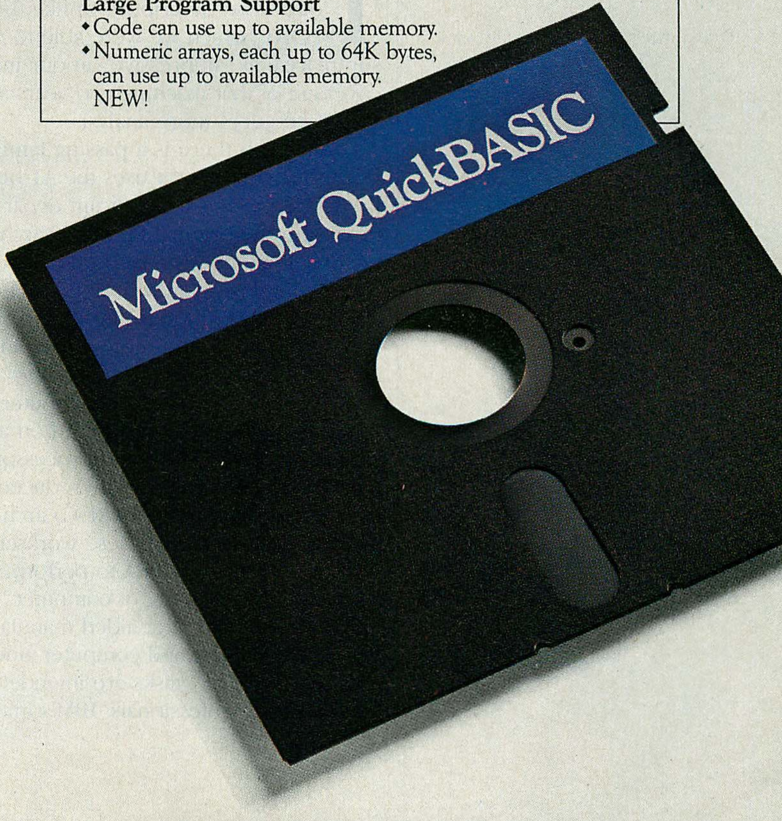
Complete Programming Environment
- Built-in Editor that places the cursor on found errors automatically. NEW!
- Compile entirely in memory at speeds up to 6000 lines per minute. NEW!
- Link routines once when starting a programming session and no need to link again when changing programs. NEW!
- Built-in debugger with single-step, animate, and trace modes. NEW!
- Create stand-alone programs.

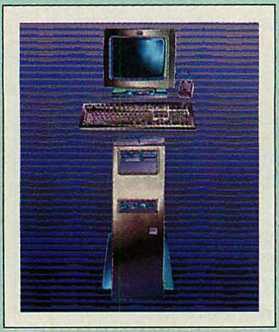
Alphanumeric Labels
- Can be used to make your programs more readable. Line numbers are not required but are supported for BASICA compatibility.

Structured Programming Support
- Block IF/THEN/ELSE/END IF eliminates the need for GOTO statements. NEW!
- Subprograms can be called by name and passed parameters. Both local and global variables are supported.

Modular Programming Support
- Separate compilation allows you to create compiled BASIC libraries to use and re-use your programs.
- A library of routines to access DOS and BIOS interrupts is supplied. NEW!

Large Program Support
- Code can use up to available memory.
- Numeric arrays, each up to 64K bytes, can use up to available memory. NEW!





RT PC: A Significant Departure

The first member in a distinct new line of microcomputers from IBM, the RT PC blends mainframe technologies with advanced desktop strategies to produce a fast and powerful, yet flexible, computing entity.

THOMAS V. HOFFMANN

The RT Personal Computer defies a one-word descriptor. Unlike the PC/AT, which we were able to summarize as "impressive" in our initial coverage of that machine two years ago, the RT requires more analysis.

Although there is a passing family resemblance in that it uses the AT bus, the RT represents a significant departure from the original PC family architecture. It is faster, more powerful, more complex—a new breed of machine. The RT's place in the IBM puzzle is an intriguing question to which an answer remains to be written.

The RT is not a single computer, but a line of workstations based on an IBM-developed 32-bit microprocessor that, in turn, is based on the reduced instruction set computer (RISC) architecture. IBM states that these workstations, the company's first to perform stand-alone processing of computer-aided design/computer-aided manufacturing (CAD/CAM) and computer-aided engineering (CAE) tasks are intended for technical professionals. IBM's initial software offerings for the RT support this statement. The operating system for the RT is derived from UNIX System V, a system well known to the technical professional. Language processors are offered for BASIC, C, FORTRAN 77, and Pascal—languages that are widely used in technical areas in business, government, and academia. Extensive graphics support is provided including a Graphics Development Toolkit and a Tektronix Graphics Terminal Emulator.

Despite this clear technical orientation, the capabilities of the RT system extend far beyond science and engineering. The RT's virtual memory management, easily replaceable 32-bit processor, high-level virtual resource manager, and comprehensive operating system provide a solid base for supporting various multitasking, multiuser applications, technical or otherwise.

The following five articles describe in detail the RT PC system as it was announced by IBM and as it may appear in the coming months if it is upgraded as the market demands.

PHOTOGRAPHS • BLAKESLEE-LANE   COMPUTER GRAPHICS • NATALE/EAST

PHOTO 1: *RT PC 6151 Model 10 System*

PHOTO 2: *RT PC 6150 Model 20 System*

Photo 1: The RT PC 6151 Model 10 is a desktop unit that features 1MB of real memory (expandable to 3MB) and a 40MB disk capacity. It is slightly larger than the AT.

Photo 2: RT PC 6150 Models 20 and 25 are floor-standing units that provide two built-in serial ports, two additional I/O adapter slots, and additional disk storage capacity.

Photo 3: The rear panel of the unit features connectors for power, the keyboard, and other external devices. Note the filters on the keyboard, mouse, and serial device cables.

Photo 4: The Models 20 and 25 system units provide eight I/O adapter slots; disk drives are mounted front and back.

Photo 5: The system speaker is mounted in the keyboard. The controller provides an audible, but defeatable, key click.

PHOTO 3: *Model 20 Rear Panel*

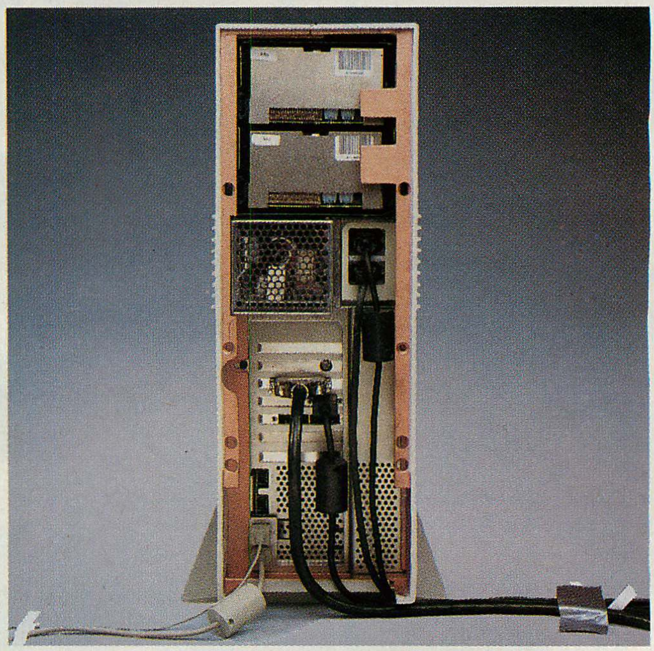


PHOTO 4: *Inside the System Unit*

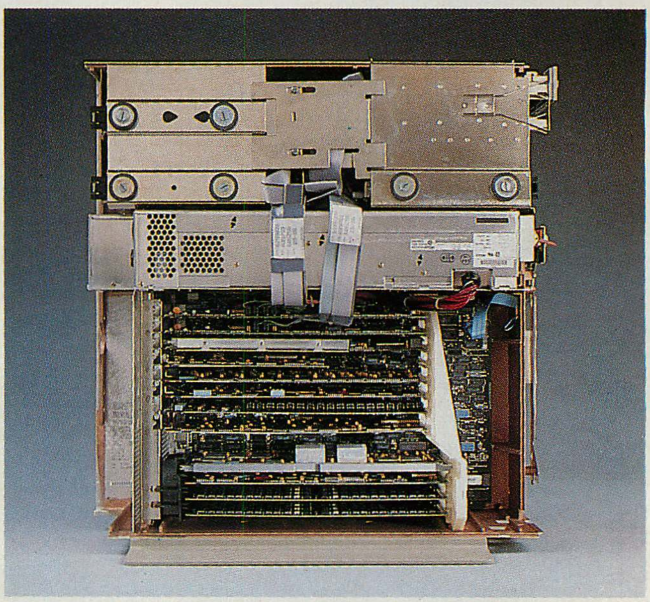
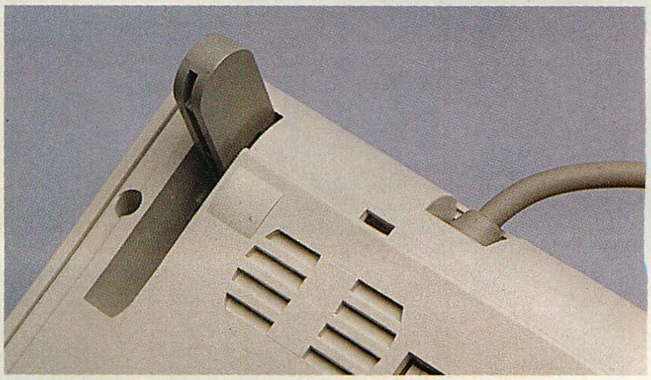


PHOTO 5: *Keyboard Underside*



This first article is an overview of the entire RT system, including the processor, memory, floating-point accelerator, displays, and mass storage devices, and the AT coprocessor. "An Architecture Apart" (p. 72) makes clear that the RT, with its support of an extremely large virtual address space and the use of a 32-bit RISC processor is altogether different from the original PC architecture. "The Insulating Layer" (p. 90) examines the Virtual Resource Manager, the sophisticated layer of high-function software that IBM has wrapped around the RT processor and its I/O devices to provide a more convenient interface than that offered at the hardware level. "The Refining of UNIX" (p. 98) describes the RT's Advanced Interactive Executive (AIX) operating system, its UNIX System V core, and the menu, windowing, and DOS-like functions included by IBM. "The Nearby AT" (p. 118) addresses the feature that most closely ties the RT to the PC family, the Personal Computer AT Coprocessor Option. This single adapter contains the essentials of a 6-MHz AT and can be used along with supporting software to run popular PC software. The software can run on the coprocessor concurrently with programs executing on the RT processor; both processors share memory, mass storage, and I/O devices.

Taken together, these articles describe a system that shares some family traits with the PC, but that introduces enough new and unique features to qualify as the beginning of a distinct new line of computers. Only time will tell if IBM provides the upgrades and enhancements needed to allow this system to realize its full potential.

RT OBJECTIVES

The original RT project objectives were to bring mainframe performance to the desktop by using the latest available technologies in computer architecture, hardware, software, and manufacturing. Several features were decided early on, including the following:

- A fast 32-bit processor
- Large primary (RAM) and secondary (disk) storage
- Virtual storage, allowing programs and data to exceed the available physical memory
- All-points-addressable graphics displays and adapters
- Multitasking operating system
- Ease of use
- Flexible open architecture

The initial products offer all of these: true 32-bit virtual memory architecture, 1MB to 4MB of main memory (with provision for up to 16MB), 40MB to 210MB of hard-disk storage, several display options, and a complete UNIX-based operating system with significant functional enhancements.

What is most interesting about the RT is the way the architecture and implementation accommodate change. The RT was designed from the beginning to be flexible and modular, which would allow major components and subsystems to be replaced without adversely affecting the rest of the system.

Examples of this design approach abound. The processor is on its own card, not on the system board, and contains its own timing logic independent of the I/O channel. Upgrading to a faster processor is a simple plug-in operation. On the software side, the Virtual Resource Manager (VRM) provides a very high-level interface to a virtual machine that manages virtual memory, physical I/O using loadable device drivers, and realtime multitasking. The AIX operating system (IBM's adaptation of UNIX for the RT) sits atop the VRM. AIX could be replaced by another operating system, without having to reimplement physical device drivers or complex memory management code.

The RT was designed to allow major components and subsystems to be replaced without adversely affecting the rest of the system.

In its current form, the RT PC shows several important influences from the PC. The I/O channel is an extended PC/AT-compatible bus that directly supports many existing adapters. Despite the unique proprietary processor, the RT's system architecture is even more open than that of the original PC family. Why? Because from the beginning, IBM is providing more and better information about *interfaces*, even though many aspects of the actual *implementation* are kept secret.

Unlike the corresponding PC family documents, the RT PC *Technical Reference* contains no ROM program listings or logic diagrams for the processor, memory, or system boards. The interface descriptions, however, are more complete and include detailed hardware timing specifications. Several third-party vendors already offer 8MB memory boards for the RT, at prices-per-megabyte significantly below IBM's initial memory offerings. Tall Tree Systems, for example, offers an 8MB board (using 80 1-megabit RAMs) for $3,995—only $500 per megabyte. (See Product of the Month, this issue, p. 29, for a discussion of "The JRAM Family" from Tall Tree, and Directions, p. 11, for a summary of RT pricing.)

Notice that the new machine is not called the PC/RT, as might be expected if it were merely the next in the PC series. The RT begins a new family of products, the first members of which happen to be PC-like. Admittedly, the decision to call the original IBM Personal Computer the IBM PC was not exactly a stroke of genius, just a good initial guess. The PC/XT (EXtended Technology) and the PC/AT (Advanced Technology) made the *T* for technology a required feature. The RT PC advances the art of product naming once again through the application of "recursive acronym technology."

RT actually stands for *R*ISC *T*echnology—RISC represents reduced instruction set computer architecture. Traditional mainframe and super minicomputer architectures generally have very large instruction sets, with many special purpose instructions for subroutine linkage, data manipulation, and arithmetic operations. Big computers seem to have an instruction for every purpose. This is fine for assembly language programmers, once they have learned all of them; very efficient programs can be written if the correct instructions are used in each situation. Conversely, choosing the best way to write a particular code sequence often is difficult when many logically equivalent ways are available. Compilers hide these problems from the high-level language programmer, but the compiler writer cannot escape. It is difficult, and therefore expensive, to produce highly optimizing compilers for machines with very complex instruction sets.

The idea behind RISC is that a simple processor with a small, but well-chosen, set of instructions can be implemented with simpler, and correspondingly faster, hardware. The resulting instruction set leaves out many operations present in traditional architectures. For example, integer multiplication and division are left as exercises for the compiler. The compiler itself, however, can be simpler, while still generating fast code, because generally fewer choices are available among alternative code generation strategies.

PHOTO 6: *Mouse Underside*

PHOTO 7: *Cartridge Tape Drive*

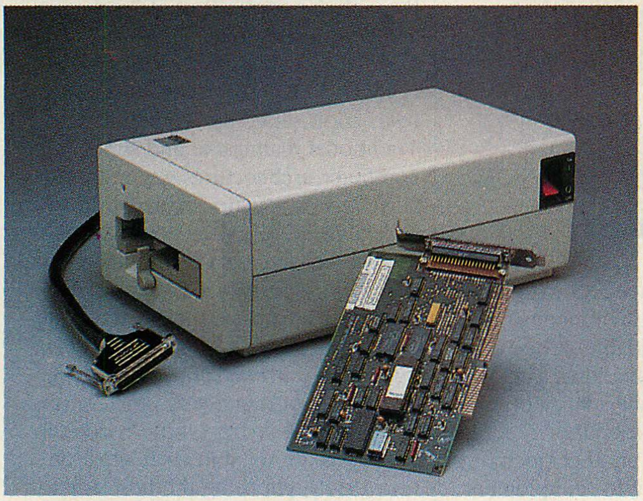


Photo 6: A two-button IBM mouse comes with the RT system. Its roller-ball tracking mechanism allows it to be used on any nearby surface. As seen here, the bottom of the mouse looks strikingly similar to that of the Microsoft Mouse.

Photo 7: The stand-alone streaming-tape drive uses standard QIC-02 one-quarter-inch cartridges with a capacity of 55MB per tape, and a data rate of 5MB per minute. This drive is also used on the IBM System/36 and IBM System/36 PC.

Photo 8: The system board has dedicated slots for the processor, floating-point accelerator, and two system memory boards. The system board for the desktop Model 10 provides six AT-compatible I/O adapter expansion slots. The system board shown above, for the floor-standing Models 20 and 25, has eight expansion slots and two RS-232 ports.

Photo 9: The RT's CPU is mounted on a separate board that plugs into the system board. The board contains the IBM-proprietary ROMP microprocessor and the memory management unit (MMU), which is an IBM-proprietary VLSI chip.

Photo 10: IBM offers a 1MB memory board in addition to the 2MB board shown on the right. Tall Tree Systems' 8MB board (on the left) allows 16MB of memory.

PHOTO 8: *System Board*

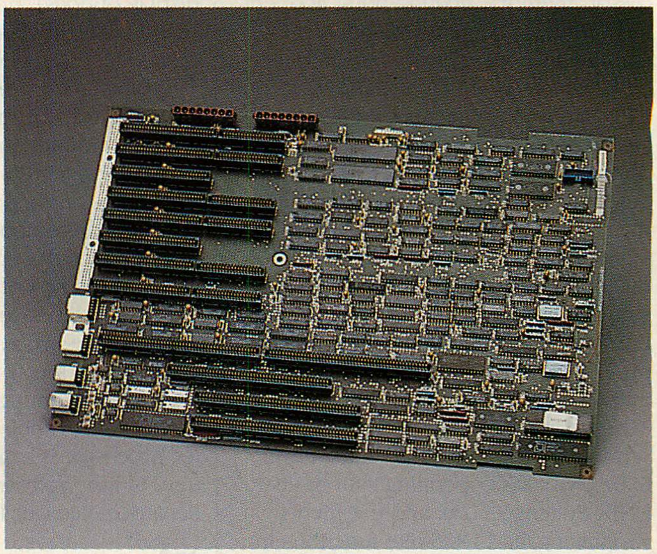


PHOTO 9: *CPU Board*

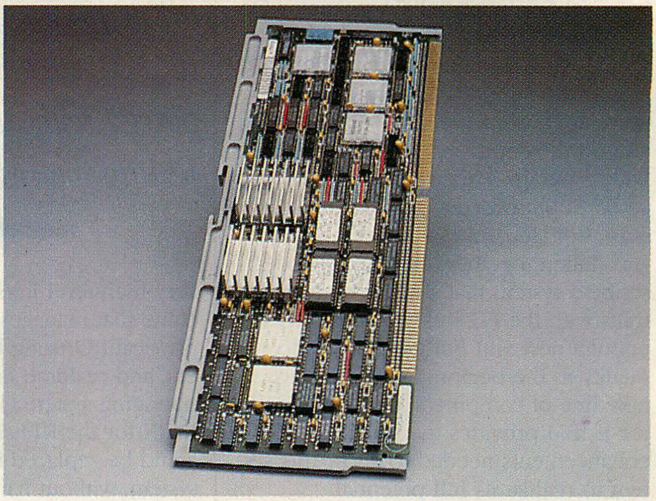
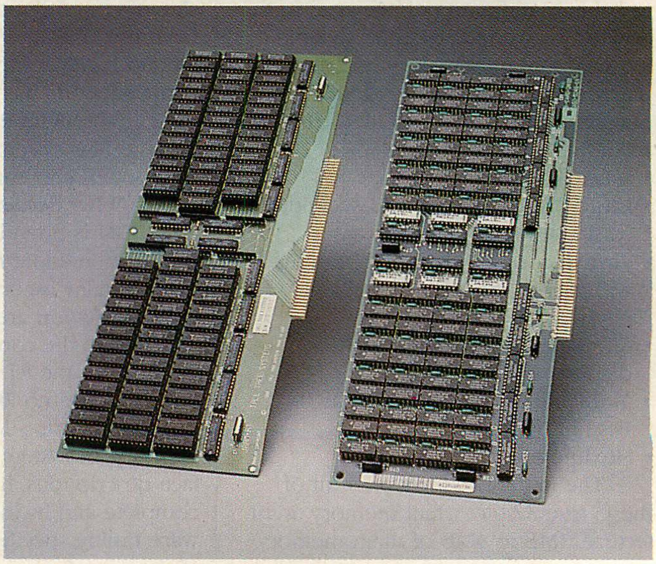


PHOTO 10: *Memory Boards*



THE BIG PICTURE

This first release from the RT PC family consists of two basic packages and three models. The 6150 Models 20 and 25 are floor-standing consoles; the 6151 Model 10 is a desktop unit, slightly larger than the AT. All models use the same processor, system memory, floating-point accelerator, and I/O adapter boards. A different system board is used in each package. The desktop unit has only six I/O adapter slots, compared to eight in the floor consoles, and lacks the two built-in RS-232 serial ports present in the larger units. The various models come with different amounts of system memory and disk storage, but are otherwise functionally identical. Table 1 lists the RT PC configurations available in this first issue of the machine.

The front panel of both RT packages has an AT-style key lock, power indicator, and a two-digit numeric display that is used to present status and diagnostic information.

System board. The RT system board provides the connections and interfacing electronics for all of the major system components, as well as the I/O subsystem. Four dedicated slots labeled A through D are for the processor, floating-point accelerator, and two system memory boards. The I/O channel slots are in addition to the four dedicated slots. (Figure 1 is a block diagram of the system board unit.)

The system board contains three channels, or data paths, each one specialized for its particular function. The memory channel is a dedicated interface between the processor and main system memory. The processor channel is a more generalized 32-bit bus of which the processor card is always master, and connects the processor to the I/O system. The 8/16-bit I/O channel is an extension of the AT I/O channel.

The memory channel connects the system memory to the processor board using a multiplexed address bus, a 40-bit data bus, and control signals. The data bus provides 32 bits of actual data plus 8 bits of error correcting code (ECC) that can correct any single-bit error and detect all 2-bit errors and many multiple bit errors. The address bus supports up to 16MB of system memory. The memory channel can transfer a full 32-bit word every 170 nanoseconds, for a memory bandwidth of 23.5MB per second.

The processor channel connects the processor board to the I/O subsystem and the optional Floating Point Accelerator card. The I/O subsystem includes the following:

TABLE 1: *RT PC Configurations*

	10	20	25
System unit/keyboard	●	●	●
Memory[a]	1MB	1MB	2MB
Hard disk/diskette adapter	●	●	●
Diskette drive (1.2MB)	●	●	●
Diskette expansion	○	1	1
Hard disk	40MB	40MB	70MB
Disk expansion	○	2	2
Expansion slots[b]			
16-bit	5	6	2
8-bit	1	2	2
Floating-point accelerator slot	●	●	●
RS-232 serial ports	○	2	2

● =Yes ○ =No

All models include clock/calendar with battery backup, hardware page-level storage protect, and security capability with standard key locks.

[a] *All models can accept one additional 1MB or 2MB memory card.*

[b] *One 16-bit slot is used for the disk/diskette adapter.*

Adapted from the IBM RTPC brochure

The desktop (10) and floor-standing (20 and 25) models come with different amounts of memory and disk storage, but are otherwise functionally identical.

- I/O channel converter (IOCC). This logic converts the 32-bit processor channel to the 8/16-bit I/O channel that is compatible with the I/O channel of the AT.
- System DMA (direct memory access) controllers. Two Intel 8237 DMA controllers provide eight channels of DMA, one of which is available only in the slot that is intended for the AT Coprocessor.
- System interrupt controllers. Two Intel 8259 priority interrupt controllers provide the system with 15 levels of priority interrupts. Additional logic implements shared interrupts, in which multiple devices may share a single interrupt level.
- Translation control logic. This logic controls the mapping of addresses from the processor's I/O channel into system memory.
- Keyboard/locator controller. An Intel 8051 microcontroller provides intelligent keyboard, locator (mouse or tablet), and speaker functions.
- Realtime clock. A Motorola 146818 CMOS clock provides a battery backed-up time-of-day clock and nonvolatile RAM. This is the same device used on the AT.
- RS-232 serial ports. RT floor-standing Models 20 and 25 provide two asynchronous serial ports, supported by a Zilog 8530 device. These serial ports support DMA transfers.

The I/O channel connects the processor (through the IOCC) to AT-compatible I/O adapters. This channel also supports several enhanced features. Shared interrupts allow multiple adapters to use the same hardware interrupt priority level. Burst and buffered DMA modes support improved DMA performance. In burst mode, an adapter can perform multiple transfers without giving up control of the bus. Buffered mode assembles two 16-bit words from the I/O channel into a single 32-bit word that is transferred to or from system memory in a single operation, thus reducing the number of main memory cycles stolen for DMA operations.

The RT keyboard introduces the new IBM standard key layout, now also available on the XT and AT. The RT version has a unique connector, in part because the keyboard contains the system speaker. The controller generates audible key clicks by default, but these can be turned off with a key combination.

Processor and memory. The processor card contains two IBM-proprietary VLSI (very large scale integration) chips, the ROMP microprocessor and a separate memory management unit (MMU). ROMP is another recursive acronym, this time for *R*esearch and *O*PD *M*icro-*P*rocessor, thus reflecting the cooperation between IBM Research and the Office Products Division in the development of the microprocessor.

The ROMP has a basic instruction cycle of 170 nanoseconds, and most instructions actually execute in one cycle. The processor system is heavily pipelined; instructions following a memory reference can be executed in parallel with the memory activity if they do not depend on data not yet read.

PHOTO 11: *Floating Point Accelerator*

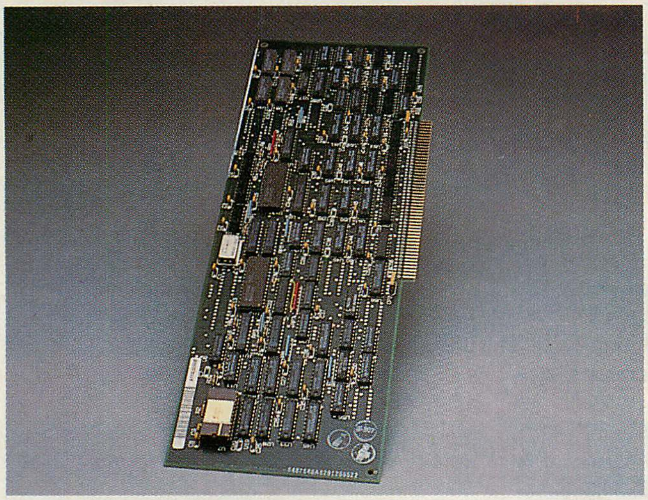


PHOTO 14: *Set-up and Installation Card*

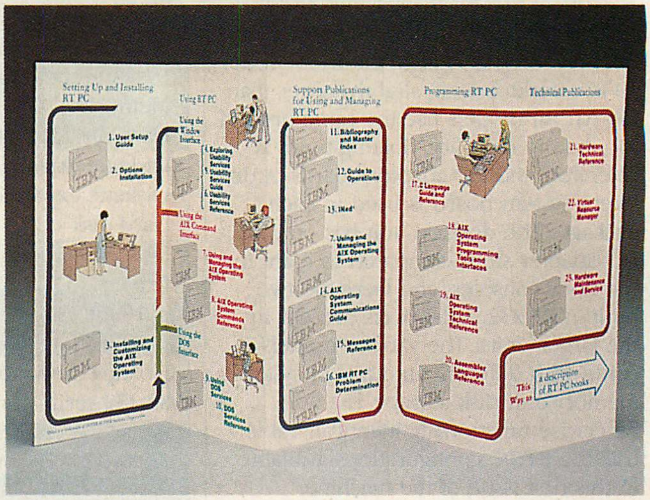


PHOTO 12: *AT Coprocessor*

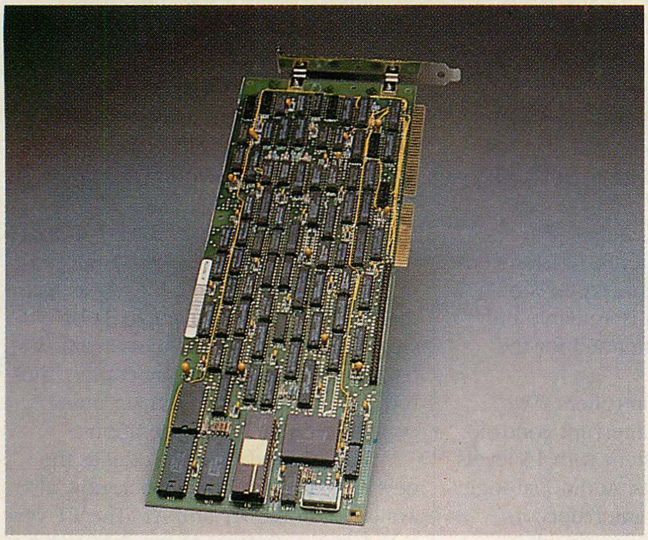


PHOTO 15: *AIX Software Manual*

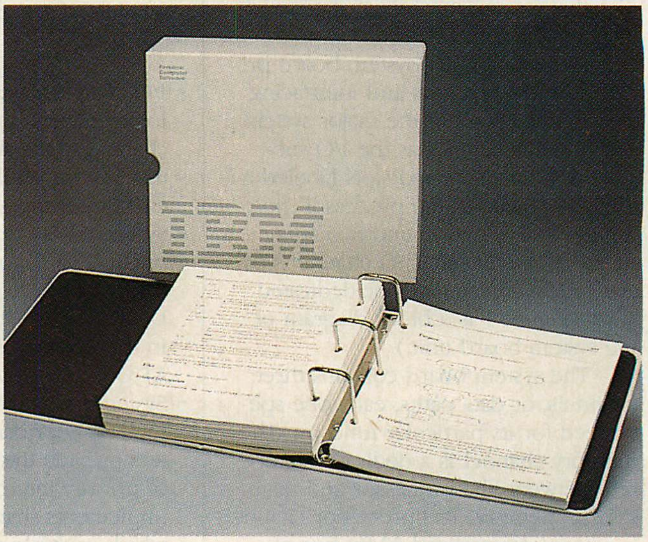


PHOTO 13: *Multiport Communications Adapter*

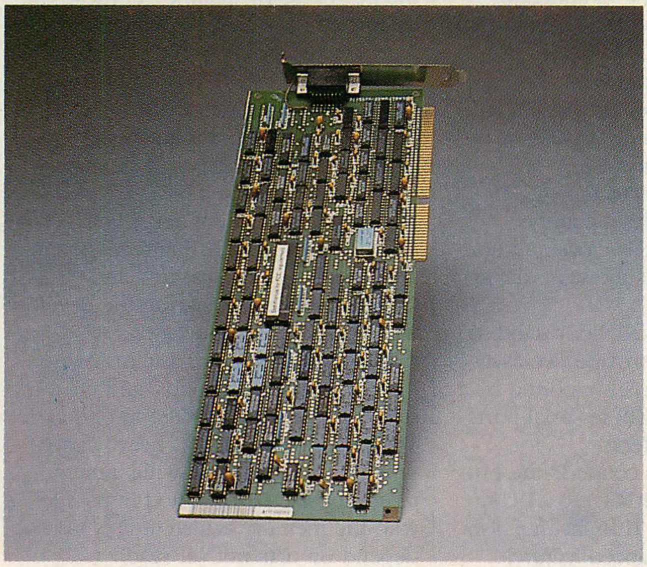


Photo 11: The Floating Point Accelerator uses a 10-MHz National Semiconductor NS32081 floating-point unit that implements a subset of the IEEE floating-point standard. It has 32 sets of sixteen 32-bit registers external to the NS32081.

Photo 12: The AT Coprocessor is a single-board version of a PC/AT that plugs into a particular slot in the I/O channel and can run existing programs written for the IBM PC family. Such programs generally run about 20-percent slower than on an actual 6-MHz PC/AT (or about 60-percent slower than an 8-MHz PC/AT).

Photo 13: The RS-232 adapter uses National Semiconductor 16450 UARTs to provide four ports through four 10-pin connectors. The connectors are the same as those for the two RS-232 ports on the Model 20 and 25 system boards.

Photo 14: The set-up and installation card provides a road map to the extensive set of manuals that describe the installation and use of the RT. It sketches the contents of the system documentation and suggests a reading sequence.

Photo 15: The manuals that accompany the RT PC break with tradition. They are printed on 8½-inch-square pages rather than the 5½-by-8½ sheets generally used.

The MMU is responsible for physical memory control, including RAM refresh, as well as virtual address translation. The ROMP generates 32-bit addresses that are converted by the MMU first into 40-bit virtual addresses, then into 24-bit physical addresses.

The processor card also has 64KB of ROM (four 16KB chips) that contain the power-on diagnostics and IPL (initial program load) programs.

System memory cards. The current implementation of the RT architecture allows for a maximum 16MB of physical system memory. The two dedicated memory card slots on the system board each can accept cards containing up to 8MB of memory. IBM currently offers only 1MB and 2MB boards, limiting total capacity to 4MB.

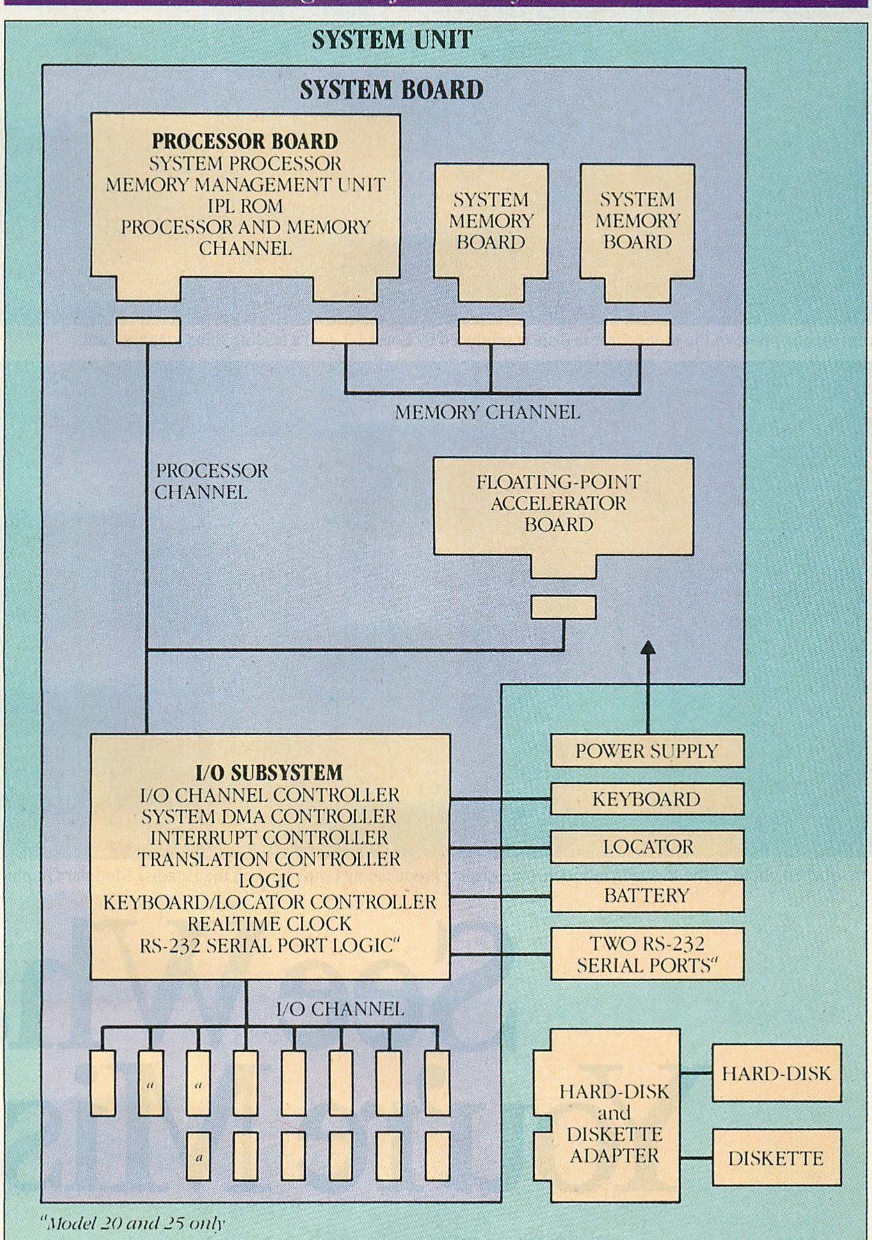
RT system memory cards are organized quite differently from those for the PC family. PC expansion memory plugs into the general-purpose I/O channel. RT memory cards are attached to the processor on a dedicated memory channel that is specially designed for fast memory access; thus, the memory cards themselves are simplified.

The RT has no switches to set to indicate memory board capacities or addressing. Five lines in the memory channel are used to provide memory board size and other information to the system board and MMU. One requirement is that when two cards of different capacities are used, the larger one must go in slot C (the first memory slot).

Each RT memory card has two independent banks of memory, each 40 bits wide (32 data bits and 8 bits of ECC). One bank contains only even-addressed words, the other only odd-addressed words. This two-way interleaving allows a full data word access every 170 nanoseconds using standard 150-nanosecond dynamic RAMs. The memory channel contains independent address and control lines for each memory bank, controlled by the MMU. The addresses on the memory channel are in the multiplexed RAS/CAS (row address strobe/column address strobe) form expected by today's industry-standard dynamic RAM chips.

This form of addressing is based on the fact that RAM chips actually contain rectangular arrays of memory cells, which are organized in rows and columns. These arrays are addressed by independently specifying a row address and column address with appropriate strobe signal. Addressing the memory cards in this way eliminates the need for logic on the cards to convert "normal" memory addresses into RAS/CAS

FIGURE 1: *Block Diagram of the RT System Unit*



Adapted from IBM RT PC Hardware Technical Reference

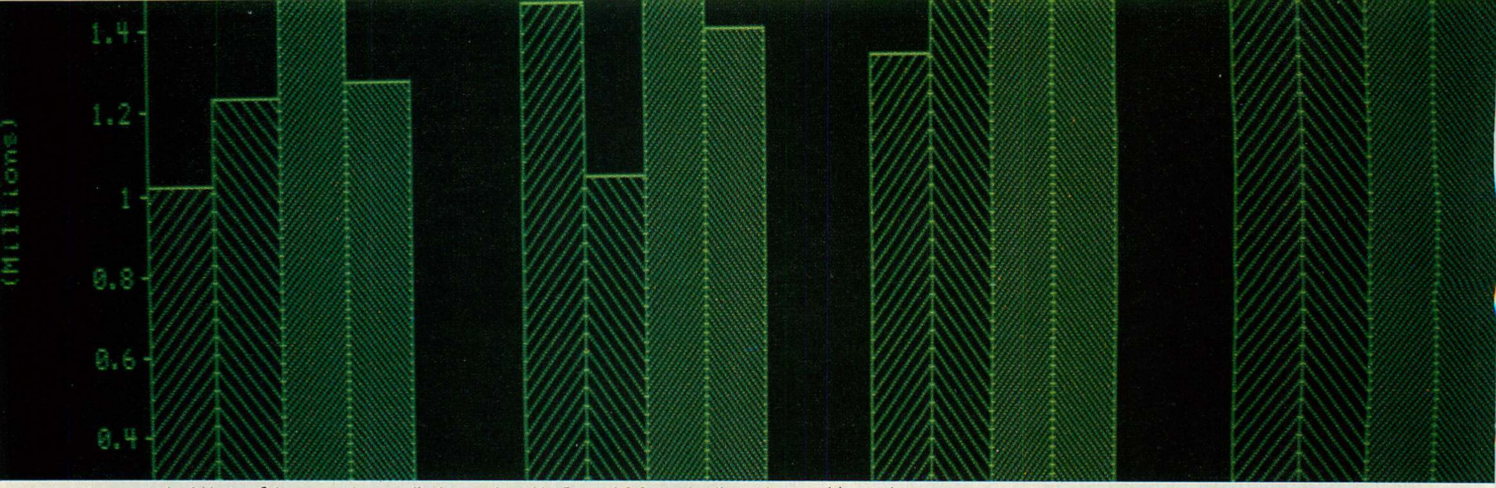
The RT system board provides the interface for the major system components: the processor, the floating point accelerator, system memory, and I/O subsystem.

form and control the associated timing. These functions, as well as ECC and refresh, are all performed on the processor card by the MMU chip.

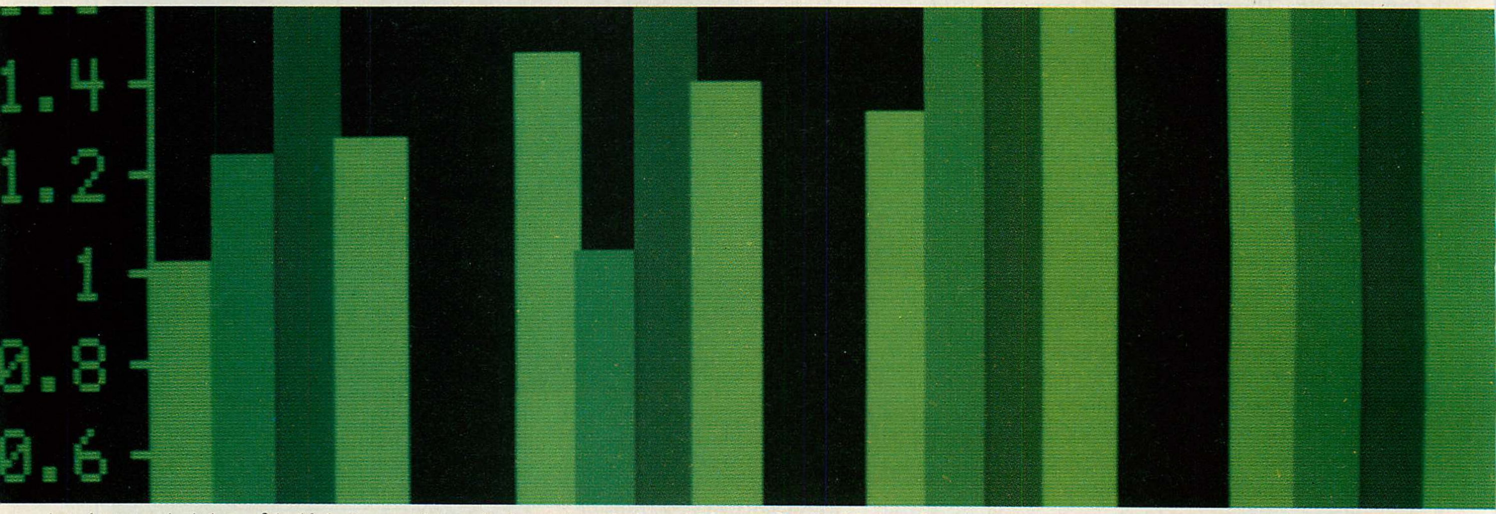
Using standard 256K-by-1 RAMs, two banks of 40 bits requires 80 RAM chips for a total of 2MB of memory, which is all the current memory board size can accommodate using standard dual in-line packages. IBM's 1MB board uses 40 64K-by-4 RAM chips, which cost a bit more than the 256K-by-1 chips.

Floating Point Accelerator. As mentioned previously, the RISC approach dictates some simple machine instructions that do not include integer multiply and divide instructions, much less floating-point operations. IBM offers an optional Floating Point Accelerator (FPA) card that plugs into a special slot (B) on the system board and attaches to the processor card via the processor channel. The FPA uses a 10-MHz National Semiconductor NS32081 floating-point unit that implements a subset of the IEEE floating-point standard. Software in the VRM floating-point driver fills in the gaps to provide the complete set of floating-point operations.

The FPA incorporates several features intended to enhance its performance in the RT system. The ROMP and



Actual unretouched photo of the monochrome display produced by Lotus 1-2-3 on a leading color graphics card.



Actual unretouched photo of the 16-shade monochrome display produced by Lotus 1-2-3 on the Paradise Modular Graphics Card.

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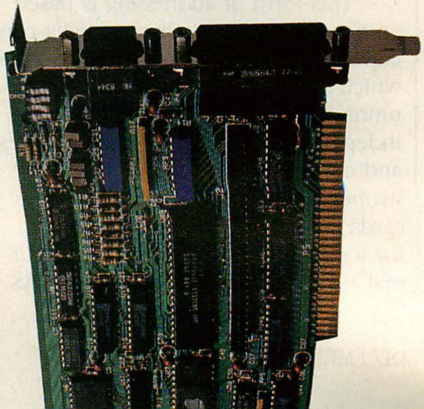

the FPA can execute in an overlapped fashion, with the FPA executing one command while the ROMP prepares the next one. In fact, the FPA actually can receive a second command while a previous command executes. The FPA has 32 sets of 16 32-bit registers external to the NS32081. Fourteen registers in each set are available for operands; the other two are for status and system use. An FPA command is available to switch register sets. It can be used by the system during a task switch instead of having to unload and reload the FPA. The 32 register sets are managed by VRM (they can only be changed in ROMP supervisor state), and can be allocated to multiple tasks within the same program as well as different programs.

IBM claims the FPA improves system performance from 12K WIPS (Whetstone instructions per second) to 125K WIPS or more.

Device support. Because the RT has an I/O channel compatible with the PC/AT, it is natural to expect that any device that works in an AT also will work in an RT. However natural this may seem, it is not true, generally because of the lack of software drivers to operate the devices. The venerable IBM Color Graphics Adapter (CGA), for example, is not supported, although the IBM Enhanced Graphics Adapter (EGA) is.

Device adapters such as the EGA, AT Fixed Disk and Diskette Adapter, and PC Network Adapter, that have on-board BIOS support programs in ROM, present a special compatibility problem. These ROMs contain device support code intended for execution on Intel 8086 family microprocessors, not the RT's ROMP. These functions have to be rewritten in device drivers that are loaded as part of the VRM.

The remainder of this overview article focuses on the major devices and adapters supported by the first release of the RT PC system software, and some scheduled for late 1986.

Mass storage. The RT supports both 5¼-inch diskette and hard-disk drives. Each RT configuration comes standard with a 1.2MB high-density diskette drive and one hard-disk drive (40MB on the models 10 and 20, and 70MB on the model 25). The 40MB systems use the standard PC/AT Fixed Disk and Diskette Drive Adapter to control the diskette drive and up to two hard disks.

The floor-standing packages have space for a second diskette drive and a maximum of three hard disks; the addition of a third hard disk would require a second controller. The second diskette can be either another 1.2MB high-density drive, or a standard 360KB drive for compatibility with standard PCs. The desktop model 10 can support only one diskette drive and one hard disk.

In August 1986, IBM announced a replacement for the originally announced 70MB hard disk for the model 25. The new disk supports the proposed ANSI-standard extended small device interface (ESDI), and requires the RT PC ESDI Magnetic Media Adapter. ESDI offers twice the disk-to-controller transfer rate (10 megabits per second) and a more noise-immune electrical interface. The new adapter provides the same diskette and hard-disk functions as the standard AT adapter, but supports the new hard-disk interface. The diskette interface did not change.

Systems with a mixture of 40MB and 70MB hard disks require two disk controllers: a standard AT controller for ST506 40MB drives and the new ESDI controller for the 70MB drives.

A streaming-tape drive and adapter are available for system backup. The drive uses standard QIC-02 one-quarter-inch cartridges, with a capacity of 55MB per tape. This is the same 6157 drive that is used on the System/36 and System/36 PC. The 6157 formats as it writes, and has a read-after-write head to detect errors while writing. IBM claims data rates to 5MB per minute are possible with this unit. Software for both file-by-file and disk-image backup and restore is provided with the standard RT system package.

The RT has an I/O channel that is compatible with the AT, but not all AT devices will work, due mainly to a lack of software drivers.

Displays. The RT supports two existing PC-family display adapters and three new all-points-addressable display adapters that were announced with the RT. The IBM Monochrome Display and Printer Adapter and the EGA are both supported by VRM device drivers.

The three new display systems for the RT are the 6153 Advanced Monochrome Display (720 by 512 pixels), the 6154 Advanced Color Display (720 by 512 pixels, with 16 colors from a palette of 64), and the 6155 Extended Monochrome Display (1,024 by 768 pixels). The 6153 and 6154 have 12-inch monitors, the 6155 has a 15-inch monitor. Only the 6153 Advanced Monochrome Display was actually available at the time that this article was written; the others should be available by the time this article is printed.

Unlike previous PC display adapters, the new ones have no on-board character generation capabilities. Everything shown on the screen is represented bit by bit in the display refresh memory, which must be written by the processor. To compensate for this extra burden in displaying text and to speed up other common bit-map operations, the new RT display adapters provide hardware assistance to reduce the work the main processor must do to manage the bit-mapped display memory.

The two smaller displays are nearly identical; the color version, however, has four parallel bit planes where the monochrome version has a single plane. Both displays use a clever memory organization that allows the processor to write any 16-bit word in a single memory operation. Without this feature, every other character in a string of 9-pixel-wide character blocks would cross a word boundary and require special processing and multiple accesses to the 16-bit wide display memory.

Additional support for pixel manipulation is provided by registers, shifters, and logic that can align, mask, and merge source data before writing to the destination display location. All of this helps make the display memory appear more uniform to the system software, so all pixels or groups of up to 16 pixels can be treated alike. This elimination of special cases at physical boundaries can greatly simplify (and therefore speed up) the software needed to perform most common display operations.

The 6155 Extended Monochrome Display adapter contains a dedicated display list processor that can execute special display commands independently of the main processor. The display processor can do rectangular area fills, copy and merge source data with destination data, perform logical operations on data, and even rotate or mirror the image being written.

The display memory organization of the 6155 carries the idea of uniform appearance one giant step further: any set of 16 either ***horizontally*** or ***vertically*** adjacent pixels can be accessed as a single 16-bit word. Thus vertical lines can be drawn just as rapidly as horizontal ones. IBM dubs this memory organization BAMDA for bit addressable multi-dimensional array.

Communications. Asynchronous communications support is available by several means for the RT PC. The standard AT Serial/Parallel Adapter is supported; it uses a single Intel 8250 UART (universal asynchronous receiver transmitter) to provide one RS-232 port through a 9-pin D-shell connector. A new four-port RS-232 adapter uses four National Semiconductor 16450 UARTs to provide four RS-232 ports through four 10-pin connectors. The system board in the floor-standing models 20 and 25 provides two RS-232 ports using a Zilog 8530 UART through the same type 10-pin connector used on the four-port RS-232 card. The new RS-422 adapter also uses NS16450 devices to provide four RS-422 ports through four 6-pin connectors. So much for standard cables.

Up to four of the four-port cards, in any combination, can be used in one system, for a maximum 18 serial devices on the floor models.

A three-port programmable multiprotocol adapter for both synchronous and asynchronous communications also should be available by the time this is printed. It uses a Zilog 8530A serial communications controller and an Intel 80C51 microcontroller and supports speeds as high as 64,000 bits per second. While three ports are provided, only two of them can be actively transferring data at the same time.

At present, this adapter is for experienced communications programmers only, because it requires *user-supplied* programming of the 8051 in order to do anything. Properly programmed, this could be an intelligent communications adapter for applications that require custom protocols, polling of remote devices, data conversion, buffering, or services that can be off-loaded to a separate communications processor.

Initial support for networks is limited to a low-level program interface to the PC Network Adapter that allows user-written applications to communicate with other PCs in a broadband network. Token-Ring Network and EtherNet adapters and supporting software also have been announced.

AT Coprocessor. The AT Coprocessor is a single-board version of an AT that plugs into a particular slot in the I/O channel and can run existing programs written for the IBM PC family. The coprocessor runs independently of the RT, although many of its functions (disk access in particular) require support from special drivers in the RT. To minimize the need for RT intervention, the coprocessor can access memory and display adapters directly in the I/O channel without going through the ROMP or memory. Programs executing on the AT Coprocessor generally run about 20-percent slower than the same program running on an actual 6-MHz AT.

THE FUTURE

To appreciate where the RT is going, it is necessary to understand from whence it came. The original IBM PC project was effected very quickly by a relatively small group of people who depended heavily on then-existing (1981) commercially available microprocessor technology. Based as it is on standard Intel processors and interfaces, the PC family as a whole has never been a place for the introduction of technology or performance significantly different from what is already widely available in the industry. Nevertheless, the PC became an instant success and as a result of its sustained success, a standard.

The RT did not come from *the PC, it came* to *the PC. It integrates large machine concepts into a small system, and in a very flexible way.*

The RT PC family is different. It is the result of a much longer and more massive development effort that began years before the PC. This was no renegade group hidden away in a closet. The RT was produced by mainstream IBMers, many of them, tucked away in a very big closet in Austin, Texas. The project manager, G. Glenn Henry, is an IBM Fellow who previously had been involved in the design of the System/3, the System/32, and especially the System/38—the innovative, single-level-storage virtual architecture of the /38 clearly influenced the RT design.

The RT did not come *from* the PC, it came *to* the PC. Its real significance is its integration of large machine architectural concepts and performance potential into a small system and in a very flexible, open-ended way. The PC-compatible I/O channel is convenient, but incidental. The 32-bit processor and virtual memory architecture are very powerful and fundamental.

What will the future bring for the RT family? Most obvious are enhancements that fit nicely into the current implementations of the RT architecture: faster processors (remember it is on a plug-in card), more memory (up to 16MB), bigger disks, more displays, networks, communications, and better software support for all of the above.

Beyond the obvious lies the uncharted realm of architecturally possible variations that must await market demands and IBM decisions to meet them. Suppose the box is enlarged to accommodate 15 or 20 adapters in the I/O channel; then departmental systems serving 30 users begin to make sense. Expanding beyond 16MB of physical memory probably would require a new MMU chip, but the memory channel contains some reserved lines that could become additional address lines, bringing the memory to 32MB or 64MB.

Now add multiple processor cards—the memory channel and MMU already have provisions for multiple MMUs; then, horizontal growth (adding capacity by adding processor elements) and fault-tolerant redundancy—and, all of a sudden, this new system offers serious computing power.

BACK TO THE PRESENT

Clone makers are going to have a much tougher time replicating the entire RT system than they did with the PC, XT, and AT, primarily because the processor and memory management chips are proprietary and available only to IBM. Yes, processors can be cloned (the NEC V20, V30, et al), but it is an order of magnitude tougher than producing dumb (in the sense of no on-board processing capability) EGA graphics cards or AT glue chips.

Furthermore, IBM has a significant advantage as the sole supplier of both the processor *and* the operating system software, in being able to include undocumented features in the processor to allow the operating system to detect, and refuse to cooperate with, ersatz processors. IBM has done it before in mainframes; it might be hard to resist the temptation to do it in the RT.

In any event, the investment needed to clone an RT is so large financially and technically that few companies (other than an IBM) could justify the effort. If the RT takes off like the AT did, however, the incentive to copy could become strong. In the meantime, opportunities abound for system builders, application developers, peripheral makers, and, of course, IBM.

Thomas V. Hoffmann, a consulting editor to this magazine, is manager of systems development for RoadNet Technologies, located in Baltimore, Maryland.

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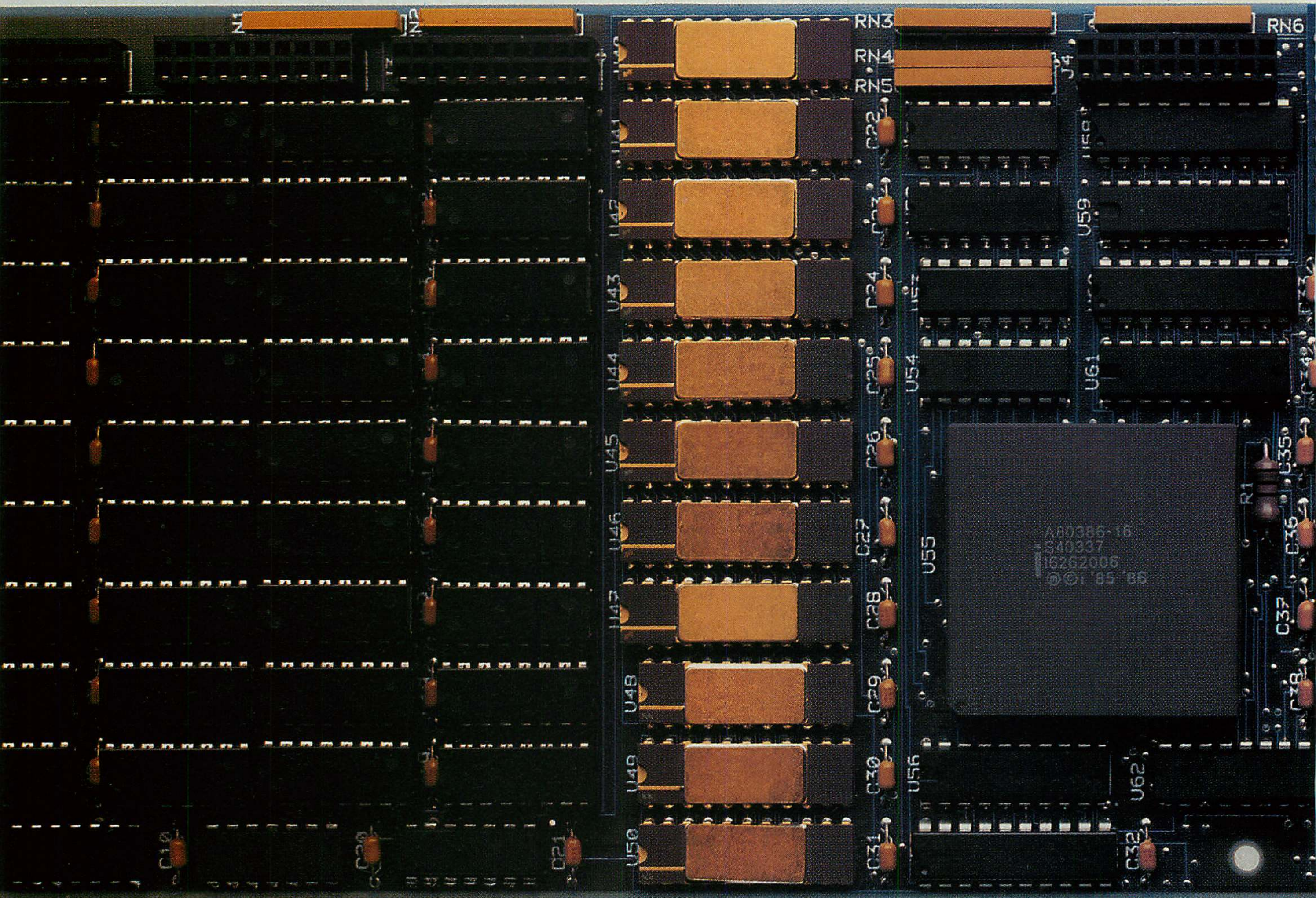

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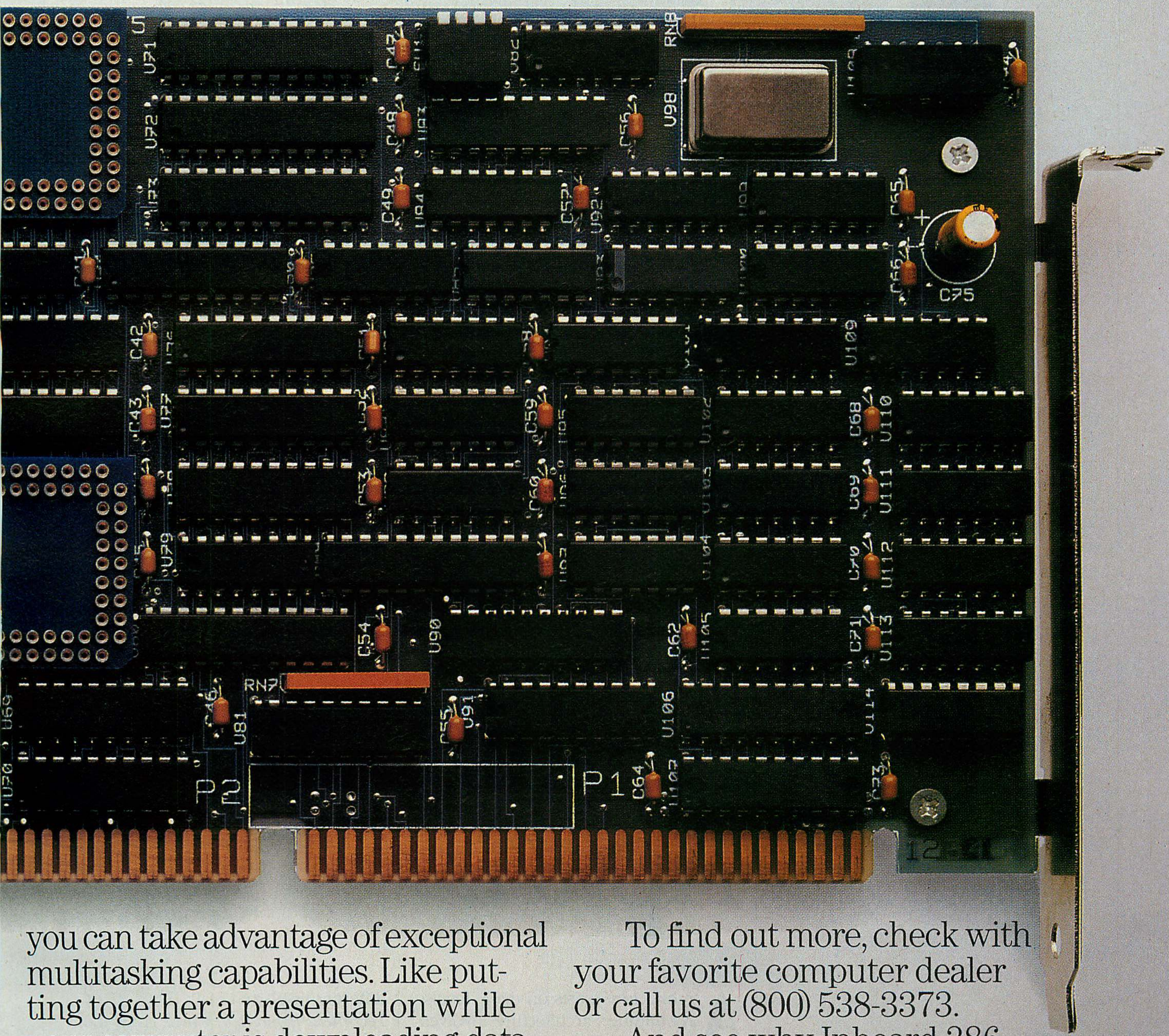

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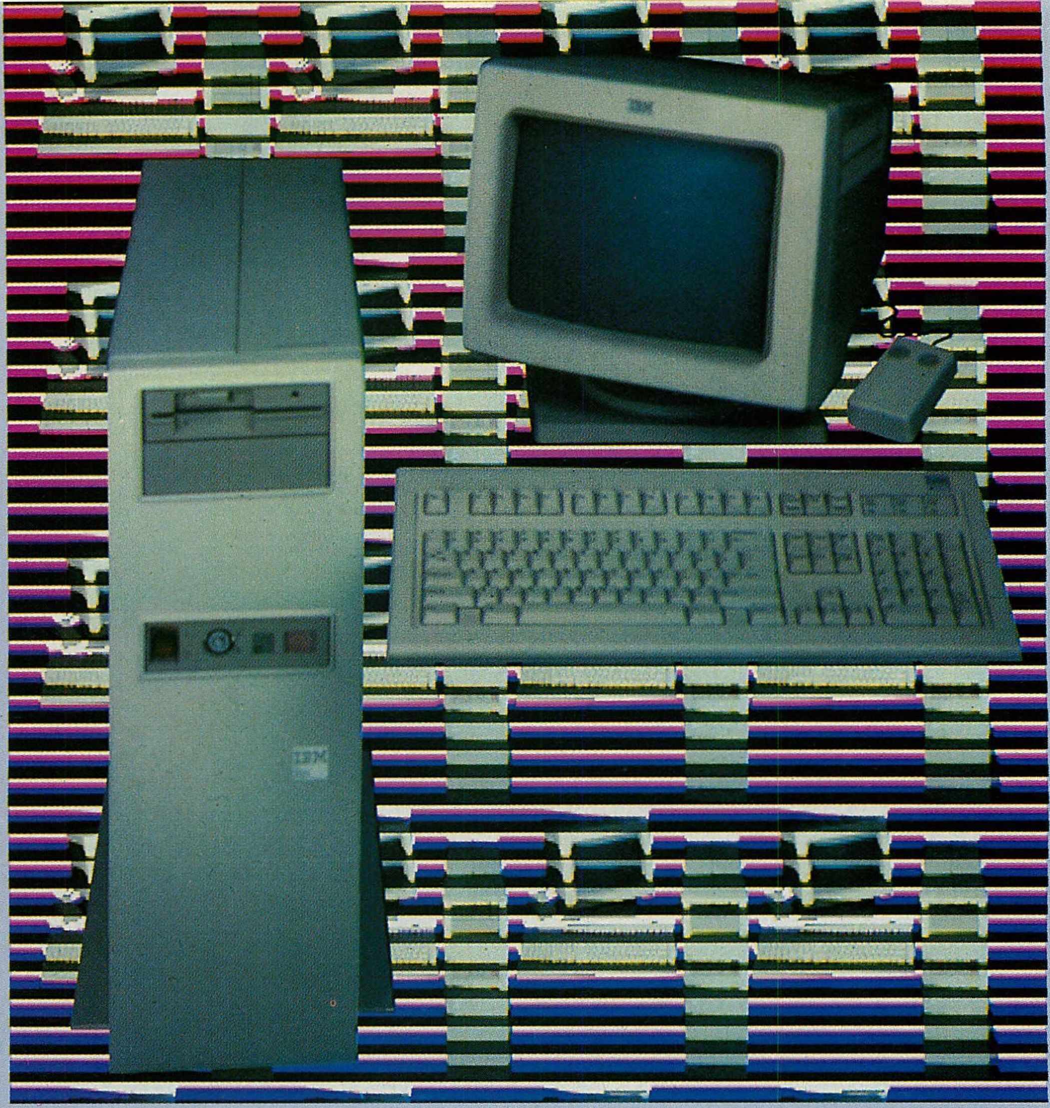

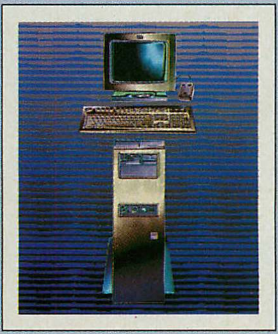

An Architecture Apart

THOMAS V. HOFFMANN

Marked by a large virtual address space and RISC processor, the blueprints for the RT differ dramatically from those for the PC.

Architecture exists on many levels. A building's architecture involves not only the arrangement of space to accommodate a human purpose, but also the innumerable details of construction, plumbing, and environmental control. Some of these details may be novel or interesting in their own right; some are just details.

Similarly, the architecture of the RT PC is quite complex, consisting of many different levels of detail. IBM's *RT PC Technical Reference*, which rivals the Manhattan telephone directory in size, takes a physical approach, fully describing each board and major functional component. This article takes a more abstract view of system features and relationships of the RT, concentrating, as it were, on the public rooms and steering clear of most of the behind-the-scenes construction details.

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The RT differs significantly from the traditional IBM PC architecture, most obviously in its support of an extremely large virtual address space and its use of a new 32-bit central processor. A more fundamental difference between the RT and PC is the degree to which hardware and software function as partners. The RT was designed and built as a *system*; the decisions about whether features should exist in hardware, software, or at all were guided by an overall set of system objectives. The fact that one person was the manager of both hardware and software development for the RT was no doubt an important factor in making this integrated system approach work.

Examples of the coordination between hardware and software abound in the RT. The processor instruction set was designed to be simple to implement in hardware, and at the same time to be a suitable target for an intelligent, optimizing high-level language compiler. The virtual memory system requires intimate cooperation from system software to deal with page faults, but the hardware is capable of searching iteratively through linked page tables in memory as part of the normal virtual address translation process. The hardware supports various kinds of memory and I/O access protection, but the decisions about what and when to protect are left to software.

ROMP SIMPLICITY

The processor in the RT is unique and proprietary to IBM; it is also likely to be the subject of many a lively discussion among would-be computer architects. Called ROMP, for research and OPD (Office Products Division) microprocessor, this is the first microprocessor in recent memory that is made simple *on purpose*. Microprocessors used to be simple because nobody knew how to make them complex. Now that we know how to make them complex, somebody wants to make them simple. *Simple*, however, does not necessarily mean easy to make or to use.

RISC (for reduced instruction set computer), the popular term for the architectural style of the ROMP, is something of a misnomer. The significance of the ROMP instruction set is not in the number and size of the instructions (118 instructions, of which 79 are two bytes long and 39 are four bytes long), but in the functions they perform and the properties they have that affect other aspects of the system.

The ROMP actually has more instructions than the 8088 (which has 87) and even the 80286 (which has 115). Unlike these Intel processors, which have one-, two-, three-, and four-byte instructions, plus segment override and repeat prefixes, the ROMP has only two instruction sizes (two and four bytes). Further, it has no fancy instructions such as MOVS, which moves string elements and increments pointers and maybe repeats all in one instruction. The ROMP does not have a specific multiply or divide instruction, although building blocks exist for them. Neither is there a stack pointer, nor, thank goodness, special index registers that get added to effective addresses.

What, then, is left for the ROMP to do? The simple answer is "nothing special." Although that is not precisely true, it captures the true spirit of RISC architecture. Generally speaking, the ROMP's sixteen 32-bit general purpose registers (GPRs) are not dedicated to a particular purpose foreseen by the architects. Contrast this with the Intel approach: AX for accumulator, BX for some indexing, BP for stack indexing, CX for counts, SI for sources, DI for destinations (and in different segments), and different segment registers for code, data, stack, and "extra."

ROMP instructions that specify registers allow the user to specify *any* of 16 GPRs. There is no accumulator, or there are 16 accumulators. There are no index registers, but there are 15 registers that can be used for indexing (R0 cannot be used because 0 means a value of 0 in instructions that take an index register). If a user wants a stack, he selects a register and increments or decrements it himself. The benefits of this approach should be quite apparent to assembly language programmers who may often find themselves needing just one more register, but not the only one that happens to be left.

The ROMP, however, was not designed for assembly language programmers—at least not human ones. The processor design was closely coordinated with the capabilities and requirements of the PL.8 compiler being developed at the same time. This compiler, which is, unfortunately, currently available only within IBM, is a very smart optimizing compiler that accepts source code in Pascal, C, and PL.8 (a PL/1 derivative for systems programming) and generates optimized object code for System/370, Motorola 68000, IBM 801 (the never-released forerunner of the ROMP), and, of course, the ROMP.

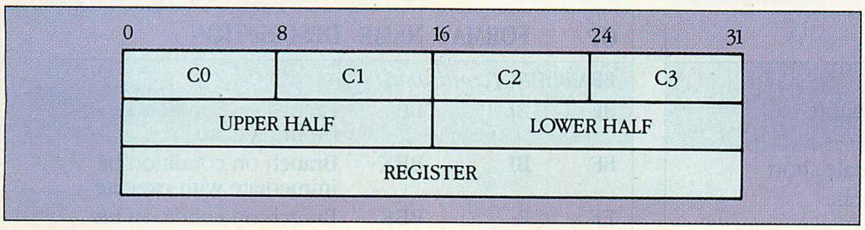
Much of the systems software for the RT was generated using the PL.8 compiler and benefits from its excellent optimization. However, the compiler delivered with the AIX operating system of the RT is based not on PL.8 but on the standard AT&T UNIX Portable C Compiler. The original release of the AIX C compiler did little optimization apart from a peephole optimizer. Version 1.1 incorporates an improved global code optimizer, based on the PL.8 compiler technology.

REGISTER MODEL

As mentioned above, the ROMP has 16 general purpose registers for use by most instructions. The contents of each register can be treated as a 32-bit quantity, two 16-bit quantities, or four 8-bit quantities (see figure 1). In addition, the ROMP has 16 system control registers (SCRs), not all of which are currently defined. SCRs 0 through 5 and SCR 9 are reserved for future versions of the ROMP. The functions of the other registers are listed below.

- SCRs 6, 7, and 8 implement the system timer facility. SCR 7 is the system timer register, which is decremented by one approximately every millisecond. SCR 8 contains status and control bits to enable a timer interrupt at a selectable priority whenever SCR 7 goes from 1 to 0. SCR 6 contains the value with which the timer is reloaded after counting down to 0.
- SCR 10 is the multiplier quotient (MQ) register, which is used in multiply and divide operations.
- SCR 11 contains the machine check status (MCS) and program check status (PCS). These registers report the reasons for special interrupts caused by hardware failures (machine check) or program exceptions (program check) such as those due to protection violations, software-initiated interrupts, and supervisor calls.
- SCR 13 is the instruction address register (IAR) that performs the same

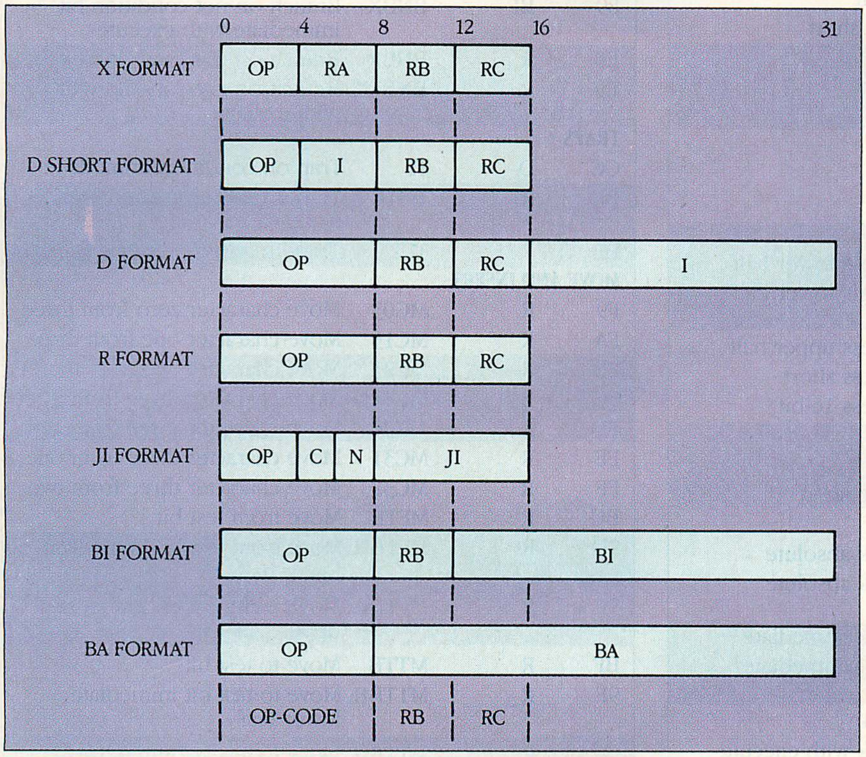
FIGURE 1: *General Purpose Registers*



Adapted from IBM RT PC Hardware Technical Reference

A general purpose register (GPR) consists of an upper and lower half of 16 bits each. It may be partitioned into four 8-bit characters: C0, C1, C2, and C3.

FIGURE 2: *ROMP Instruction Formats*



Adapted from IBM RT Personal Computer Technology

ROMP instructions are divided into seven formats according to usage of registers and memory. Any GPR may be used in instructions that specify registers.

function as the program counter (PC) or instruction pointer (IP) registers in other processors: it points to the next instruction to be executed.

- SCRs 14 and 12 are the interrupt control status (ICS) and interrupt request buffer (IRB), respectively. The ICS contains the processor priority, interrupt mask, and control bits for processor privilege state, memory protection, and translation enable. A current register set number field also is available, providing for up to eight sets of 16 GPRs, but the current implementation has only one set of GPRs.
- SCR 15 contains the condition status bits, which are set according to the results of arithmetic and shift instructions and can be tested by conditional jump and branch instructions.

ROMP INSTRUCTIONS

The 118 ROMP instructions are divided into ten classes according to function (see table 1) and into seven formats, as shown in figure 2. The majority of instructions are R-format, two-operand, register-to-register operations, which execute in a single 170-nanosecond cycle. The sole X-format instruction is CAS (compute address short), which adds two 32-bit registers and then places the result in a third, without affecting the condition bits.

D-format instructions come in both a long and a short form; the difference between the two is the size of the immediate operand field. A typical D-format instruction is ST (store), which stores a 32-bit register at the memory location addressed by the contents of another GPR and the sign-extended value of the immediate field.

The JI format is used only for the JB (jump on condition bit) and JNB (jump on not condition bit) instructions. The BA format is for absolute branches that can reference the first 16MB of segment 0 in the processor's (virtual or real) address space. The BI format is for relative branches, with a range of ± 512KB.

The 10 categories of the ROMP instruction set, listed in table 1, perform the following functions:

- The memory access instructions provide for loading and storing full 32-bit words, 16-bit half-words, and 8-bit characters. Included in this group of seventeen instructions is a test and set instruction that is useful for interprocess coordination.
- The eight address computation instructions do not affect the condition codes and are useful for computing source and destination addresses in the middle of computations, as well as arithmetic operations where the condition status of the result is not going to be tested by a branch.
- The branch instructions come in two varieties: nine ordinary branches and seven branches with execute. The latter executes the instruction immediately following the branch instruction (called the *subject instruction*) regardless of whether or not the branch is taken, just as if it preceded the branch. The subject instruction has no effect on the branch decision, which has already been made by the time the subject instruction executes. In cases where the branch is taken, the execution of the subject instruction is overlapped with the fetching of the branch target. This allows for explicit use of the pipelined architecture of the ROMP to do useful work during what would be wasted time in most processors. The branch and link instructions of this group store a return address in a designated GPR and are the basis for subroutine calls.
- The three available traps cause a program check interrupt if at least one of the specified conditions is true. The traps are generally used to detect subscript range errors, overflow, and similar conditions.
- The move and insert group provides for moving any of the four characters in one GPR to any position in another, or the same, GPR. Instructions for moving bits are also included in this thirteen-member group.
- The twenty-one arithmetic instructions consist of the usual group, except that

TABLE 1: *ROMP Instruction Set*

OP	FORMAT	NAME	DESCRIPTION
MEMORY ACCESS			
4	DS	LCS	Load character short
CE	D	LC	Load character
5	DS	LHAS	Load half algebraic short
CA	D	LHA	Load half algebraic
EB	R	LHS	Load half short
DA	D	LH	Load half
7	DS	LS	Load short
CD	D	L	Load
C9	D	LM	Load mutliple
CF	D	TSH	Test and set half
1	DS	STCS	Store character short
DE	D	STC	Store character
2	DS	STHS	Store half short
DC	D	STH	Store half
3	DS	STS	Store short
DD	D	ST	Store
D9	D	STM	Store multiple
ADDRESS COMPUTATION			
C8	D	CAL	Compute address lower half
C2	D	CAL16	Compute address lower half 16-bit
D8	D	CAU	Compute address upper half
6	X	CAS	Compute address short
F3	R	CA16	Compute address 16-bit
91	R	INC	Increment
93	R	DEC	Decrement
A4	R	LIS	Load immediate short
BRANCHING			
8A	BA	BALA	Branch and link absolute
8B	BA	BALAX	Branch and link absolute with execute
8C	BI	BALI	Branch and link immediate
8D	BI	BALIX	Branch and link immediate with execute
EC	R	BALR	Branch and link
ED	R	BALRX	Branch and link with execute
08-0F	JI	JB	Jump on condition bit
BRANCHING *(continued)*			
8E	BI	BB	Branch on condition bit immediate
8F	BI	BBX	Branch on condition bit immediate with execute
EE	R	BBR	Branch on condition bit
EF	R	BBRX	Branch on condition bit with execute
00-07	JI	JNB	Jump on not condition bit
88	BI	BNB	Branch on not condition bit immediate
89	BI	BNBX	Branch on not condition bit immediate with execute
E8	R	BNBR	Branch on not condition bit
E9	R	BNBRX	Branch on not condition bit with execute
TRAPS			
CC	D	TI	Trap on condition immediate
BD	R	TGTE	Trap if register greater than or equal
BE	R	TLT	Trap if register less than
MOVE AND INSERT			
F9	R	MC03	Move character zero from three
FA	R	MC13	Move character one from three
FB	R	MC23	Move character two from three
FC	R	MC33	Move character three from three
FD	R	MC30	Move character three from zero
FE	R	MC31	Move character three from one
FF	R	MC32	Move character three from two
BC	R	MFTB	Move from test bit
9D	R	MFTBIL	Move from test bit immediate lower half
9C	R	MFTBIU	Move from test bit immediate upper half
BF	R	MTTB	Move to test bit
9F	R	MTTBIL	Move to test bit immediate lower half
9E	R	MTTBIU	Move to test bit immediate upper half

The ROMP implements 118 instructions; most are R-format, register-to-register operations that execute in a 170-ns cycle.

divide and multiply are missing. In their place, the ROMP has primitive instructions that perform partial divide or multiply one or two bits at a time. Library routines can use these to do normal operations. Optimization is also possible in many situations, given knowledge of the actual or maximum values of the operands.

- Logical instructions are the usual And, Or, and Xor, with the mainstream IBM mnemonics *N*, *O*, and *X*. There are sixteen logical instructions.
- The fifteen instructions of the shift group include a unique, nondestructive set of shifts in addition to the normal ones. The so-called *paired shifts* treat the 16 GPRs as 8 pairs (0 and 1, 2 and 3...). The specified register is shifted and the result is stored in its *twin* (the other member of the pair), which leaves the original register unmodified.
- The seven system control instructions manipulate the system control registers and are generally privileged. If executed with the processor in unprivileged state, a program check occurs. Operations on the MQ or condition status SCRs, however, are not privileged. The LPS (load program status) instruction loads the IAR, ICS, and CS from the designated memory location. It can be used to return from an interrupt. LPS is a privileged instruction. The SVC (supervisor call) instruction is not privileged. SVC causes a program check interrupt and is the normal way to invoke operating system services.
- Only two I/O instructions are included in the ROMP instruction set: IOR (I/O read) and IOW (I/O write). They are used to transfer data between the ROMP and the memory management unit (MMU) registers, including the segment control registers. Although the I/O instructions are not privileged, the MMU will report a protection violation if it is accessed by I/O instructions when the processor is in unprivileged mode.

PRIORITY INTERRUPTS

The RT implements a priority interrupt mechanism. The processor priority field in the interrupt control status register

OP	FORMAT	NAME	DESCRIPTION
ARITHMETIC			
E1	R	A	Add
F1	R	AE	Add extended
D1	D	AEI	Add extended immediate
C1	D	AI	Add immediate
90	R	AIS	Add immediate short
E0	R	ABS	Absolute
F4	R	ONEC	Ones complement
E4	R	TWOC	Twos complement
B4	R	C	Compare
94	R	CIS	Compare immediate short
D4	D	CI	Compare immediate
B3	R	CL	Compare logical
D3	D	CLI	Compare logical immediate
B1	R	EXTS	Extend sign
E2	R	S	Subtract
B2	R	SF	Subtract from
F2	R	SE	Subtract extended
D2	D	SFI	Subtract from immediate
92	R	SIS	Subtract immediate short
B6	R	D	Divide step
E6	R	M	Multiply step
LOGICAL OPERATIONS			
99	R	CLRBL	Clear bit lower half
98	R	CLRBU	Clear bit upper half
9B	R	SETBL	Set bit lower half
9A	R	SETBU	Set bit upper half
E5	R	N	And
C5	D	NILZ	And immediate lower half extended zeroes
C6	D	NILO	And immediate lower half extended ones
D5	D	NIUZ	And immediate upper half extended zeroes
D6	D	NIUO	And immediate lower half extended ones
E3	R	O	Or
C4	D	OIL	Or immediate lower half

OP	FORMAT	NAME	DESCRIPTION
LOGICAL OPERATIONS *(continued)*			
C3	D	OIU	Or immediate upper half
E7	R	X	Exclusive or
C7	D	XIL	Exclusive or immediate lower half
D7	D	XIU	Exclusive or immediate upper half
F5	R	CLZ	Count leading zeroes
SHIFTS			
B0	R	SAR	Shift algebraic right
A0	R	SARI	Shift algebraic right immediate
A1	R	SARI16	Shift algebraic right immediate plus 16
B8	R	SR	Shift right
A8	R	SRI	Shift right immediate
A9	R	SRI16	Shift right immediate plus 16
B9	R	SRP	Shift right paired
AC	R	SRPI	Shift right paired immediate
AD	R	SRPI16	Shift right paired immediate plus 16
BA	R	SL	Shift left
AA	R	SLI	Shift left immediate
AB	R	SLI16	Shift left immediate plus 16
BB	R	SLP	Shift left paired
AE	R	SLPI	Shift left paired immediate
AF	R	SLPI16	Shift left paired immediate plus 16
SYSTEM CONTROL			
B5	R	MTS	Move to SCR
96	R	MFS	Move from SCR
95	R	CLRSB	Clear SCR bit
97	R	SETSB	Set SCR bit
D0	R	LPS	Load program status
F0	R	WAIT	Wait
C0	D	SVC	Supervisor call
INPUT/OUTPUT			
CB	D	IOR	I/O read
DB	D	IOW	I/O write

determines whether the processor will honor a pending interrupt request. Only interrupts with a priority greater than the current processor priority are processed; interrupts of equal or lower priority remain pending.

Interrupts are honored between instructions (but not between branch with execute and the subject instruction or between LPS and the target instruction) and can arise from three sources: software-generated interrupts caused by setting bits in the interrupt request buffer; system components on the processor channel (such as the MMU and the I/O channel converter); and I/O adapters on the I/O channel.

The processor recognizes five different levels of external interrupts, plus two I/O trap levels (see table 2). The traps are for memory management hardware errors and for the power fail early warning. Both traps cause a machine check interrupt to take place.

When the processor recognizes an interrupt request, it initiates a program status (PS) exchange. The current PS (IAR, ICS, and CS) is stored in a fixed real memory location, depending on the level of interrupt source, then a new PS is loaded from the words following the old PS save area. Interrupt routines return to the previous processing level by executing an LPS instruction specifying the address of the previously saved processor status.

The eleven interrupt levels in the I/O channel, plus four more from devices on the system board, are mapped into two processor interrupt levels. System software can check the 8259 interrupt controllers to determine the specific source of the interrupt.

VIRTUALLY UNLIMITED MEMORY

The RT system supports an extremely large virtual memory, with a 40-bit virtual address. Remember that the Intel 8088 used in the PC and PC/XT has a 20-bit address, yielding a megabyte address space. The RT's 40-bit virtual address covers a mega-megabyte, or terabyte—that is, 100,000 10MB disks.

The idea behind virtual memory is that programs can access memory as a single uniform array without regard to the amount of physical memory actually

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TABLE 2: *RT System Processor Interrupts*

LEVEL	ASSIGNMENT
0	System attention sequence from keyboard
1	Realtime clock interrupt
2	IOCC errors / MMU program check
3	I/O channel interrupts (8259 #1)
4	I/O channel interrupts (8259 #2)
Trap	MMU machine check / Early power-off warning

The system processor supports five external interrupt levels, as well as a trap. IRQs from the I/O channel are connected to levels 3 and 4 through two 8259 interrupt controllers that are located on the system board.

present or available. If a program tries to access a part of the virtual memory that is not represented by a part of physical memory, a page fault interrupt occurs and the system software can read the required page from secondary storage (usually disk).

The RT processor deals in 32-bit addresses, thus giving it the ability to address 4GB (gigabytes) of memory directly. The MMU accepts 32-bit addresses from the processor (or I/O channel), but is capable of addressing only 16MB of physical memory using 24 address bits. The MMU must first translate the 32-bit virtual address into a full 40-bit virtual address before it can find the real memory that corresponds to the desired virtual location. Only then can the transfer take place. If no real memory is associated with the given virtual address, then the system software has to be notified.

To the executing program, memory appears to occupy 4GB, divided into 16 segments of 256MB each. The complete virtual space contains 4,096 segments. The 32-bit program addresses are expanded to full 40-bit virtual addresses by the MMU, which uses the high-order 4 bits of the 32-bit address to select one of 16 segment registers. The 12-bit segment number (called the segment ID or SID) contained in the segment register is concatenated with the lower 28 bits of the program address to form the 40-bit virtual address (see figure 3).

The segment registers are part of the process state maintained by the operating system. Each process, or program, can address only those segments assigned to it by the operating system. The system can permit sharing of segments by several programs by placing the same SID value into a segment register for each program.

After the MMU has translated the 32-bit address into a full 40-bit virtual address, the virtual address must be associated with a piece of physical memory. The system divides memory into pages of 2,048 bytes each. (Actually, the hardware supports either 2KB or 4KB pages, but the current software uses only the smaller page size.) A 16MB system has 8,192 pages. An inverted page table (IPT) in memory contains an entry for each real memory page. The IPT entry contains the 29-bit virtual page number (the 12-bit segment number concatenated with the 17-bit virtual page index) associated with each real page, bits that indicate whether the corresponding real page is actually assigned, and links to subsequent entries.

To avoid searching the entire IPT for each memory reference (obviously, this would be unacceptably slow), the MMU implements a hashing algorithm that generates a real page number from the virtual page number. This page number indexes a memory-resident table called the hash anchor table, which contains pointers to the corresponding IPT entry for the designated real page. The IPT is searched from that point, following the links to subsequent entries with the same hash value. Eventually, the desired virtual page is found, or the page is not present and a page fault interrupt is generated.

To optimize virtual address translation even further, the MMU contains a 32-element translation look-aside buffer (TLB) that contains the virtual-to-real correspondence for recently translated addresses (see figure 4). This on-chip cache is an associative memory, or content-addressable memory, organized as two 16-entry tables. The two tables are indexed in parallel using the lower four bits of the desired virtual page. The upper 25 bits of the page number are then compared with the contents of the TLBs. If either TLB produces a match and the TLB entry is marked as valid, then the 13-bit real page number is used directly. If the address is found in the TLB, the MMU can complete the transfer in a single 170-nanosecond cycle. If the TLB look-up fails, the IPT is searched and the results are stored in the TLB for future accesses.

When a successful virtual-to-real translation occurs, the MMU automatically updates the appropriate bits in the reference/change array located on the processor board. These bits record the status of each page of real memory and are accessible by the operating system. They are helpful in managing the use of real memory; for example, pages that are changed must be written to disk if they are to be used for a different virtual page.

In the event of a page fault, the operating system must read the desired virtual page from disk into a real page and enter the appropriate information into the IPT. The MMU then can repeat the access. The system needs a way to associate virtual pages with disk blocks. The RT's Virtual Resource Manager (VRM) uses the external page table (XPT) for this purpose. The VRM imposes a limit of 512 segment IDs (or one-eighth of the theoretical limit of 4,096) in order to keep the size of the XPT manageable. Even so, 512 segments of 128K pages each adds up to 64 mega-entries. If each entry contains a 4-byte disk block address, the XPT requires 256MB, or one whole segment, without considering the rest of the pages it represents, which require 2,048 *times* the space of the XPT. Clearly, the RT's 40-bit virtual address space leaves plenty of growing room.

MEMORY PROTECTION

The RT provides several levels of memory protection in the MMU. Each segment register contains a segment present bit. If this bit is cleared, then the MMU ignores all accesses to this segment. This feature is used not only for protection against references to unallocated segments, but also to implement memory-mapped I/O. Segment 15 is marked not present by the system software, so the MMU ignores it, and the I/O channel converter (IOCC) hardware on the system board responds only to addresses in segment 15. Therefore, all access to the I/O channel is through memory references in segment 15.

Two more bits in the segment register allow individual enabling or prohibiting of access to segments by the processor or the I/O channel. Thus, a segment can be made available to the processor, the I/O channel, both, or neither. Protection violations and page faults cause special processor interrupts.

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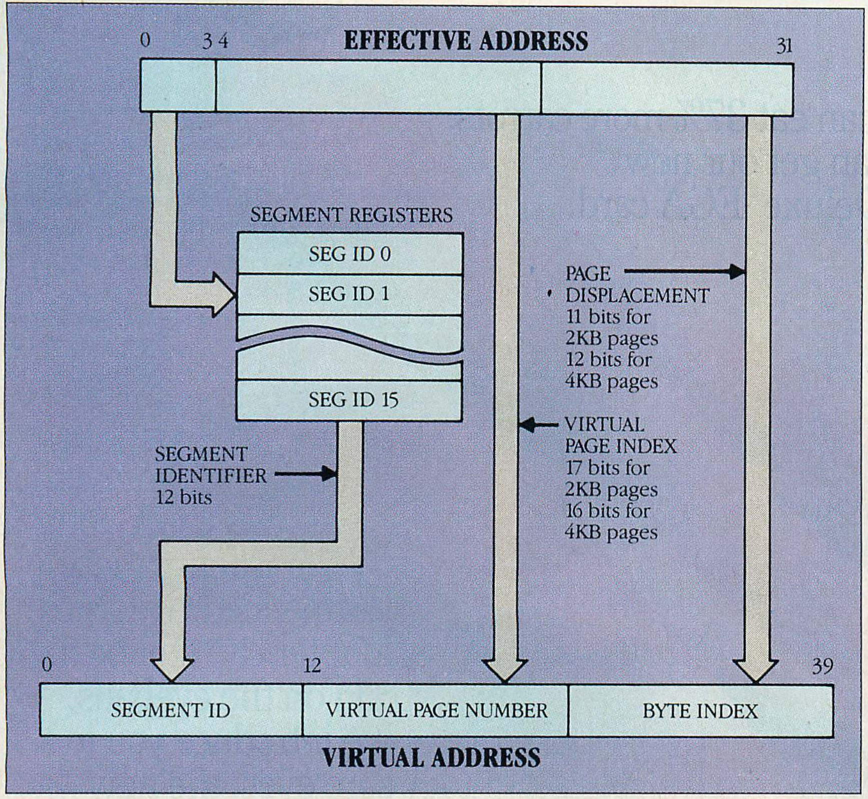
FIGURE 3: *Generation of Virtual Address*



Adapted from IBM RT PC Hardware Technical Reference

The 12-bit segment number is concatenated with the lower 28 bits of program addresses in order to form 40-bit virtual addresses.

ual pages have a two-bit key field in their ITP and TLB entries; the field defines the page type as Key-0 fetch-protected, Key-0 read/write, public read/write, or public read-only. A one-bit key in each segment register gives a process either Key-0 or Key-1 access to the pages in that segment. Key-0 privilege allows read/write access to all but public read-only pages, which are always read-only. Key-1 privilege cannot read Key-0 fetch-protected pages and can only write to public read/write pages.

Special segments, designated by yet another bit in the segment register, provide for locking of 128-byte lines according to an 8-bit transaction identifier (TID). Each ITP and TLB entry contains 16 lockbits for each page (one for each line), a TID, and a write bit. The MMU also contains a current TID register that the operating system updates each time it dispatches a process to execute. The MMU allows access only to special segment pages by processes with the correct TID. The lockbits and write bit for the page determine the type of access allowed. If the write bit is 1, locked lines can be read or written and unlocked lines are read-only. If the write bit is 0, locked lines can be read and no other access is permitted.

Interrupts caused by protection violations can be used by the operating system to control resources, implement signals, make processes wait, or detect actual violations or software errors.

I/O CHANNEL

The I/O channel (IOC) of the RT is essentially the same as that used in the PC/AT. It supports both 8- and 16-bit devices, DMA transfers, and interrupts, as well as 16-bit I/O device addresses and 24-bit memory addresses. Some adapters have only device addresses, some only memory addresses, and some (like display adapters) have both. Signals in the IOC tell the adapters whether the access is to the I/O or memory space.

One slot in the IOC, for IBM's AT Coprocessor Option, is slightly special. This slot has access to an eighth DMA channel dedicated for coprocessor use and does not support memory refresh.

The IOC is connected to the RT processor and MMU by the IOCC. The IOCC, processor, and MMU are connected to each other by a 32-bit bus called the ROMP storage channel (RSC). Transfers on the RSC are always 32 bits, as are the addresses. The IOCC must be able to recognize when RSC transfers address the I/O system and then translate them into the correct addressing and signals used on the IOC.

The IOCC accesses system memory through the MMU by originating its own transfers with either the system DMA controllers or the so-called alternate controllers. Alternate controllers are simply boards in the IOC that have the ability to generate their own addresses and cause bus transfers. They may have their own DMA controllers or even intelligent processors. The AT coprocessor functions as an alternate controller.

The IOCC is built to recognize 32-bit addresses to segment 15 as belonging to the IOC. The system software programs the MMU to ignore all segment 15 addresses. The IOCC maps the first 64KB of segment 15 (addresses F000 0000H through F000 FFFFH) to the I/O device map of the IOC, and the fifth 16MB of segment 15 (addresses F400 0000H through F4FF FFFFH) to the memory map of the IOC. Native I/O devices on the system board, such as the system DMA, interrupt controllers, and realtime clock, as well as the optional floating-point accelerator, are also addressed through segment 15.

The 16MB memory map on the IOC is completely independent of the 16MB system memory. In fact, given enough slots and sufficiently dense memory cards, approximately 13MB of memory can be installed in the IOC in addition to the 16MB of system memory. (Channel memory in excess of 13MB is reserved for the RT PC Advanced Monochrome Graphics Display and other system uses.) The channel memory would, of course, be confined to segment 15.

Aside from device adapters that incorporate memory, such as display controllers, the main reason for placing memory in the IOC is to improve the performance of the AT coprocessor. The coprocessor, or any alternate controller, can directly access both devices and memory in the IOC without going through the IOCC. However, the coprocessor should have access to system memory in a transparent way. In other words, the program executing in the coprocessor should be able to address its own 16MB logical address space without regard to whether the physical memory is located in system memory or in the I/O channel.

The system board contains logic to support the translation of addresses generated on the IOC by system DMA controllers and alternate controllers into either system memory or IOC addresses. This translation is accomplished by a 1K-by-16-bit RAM array

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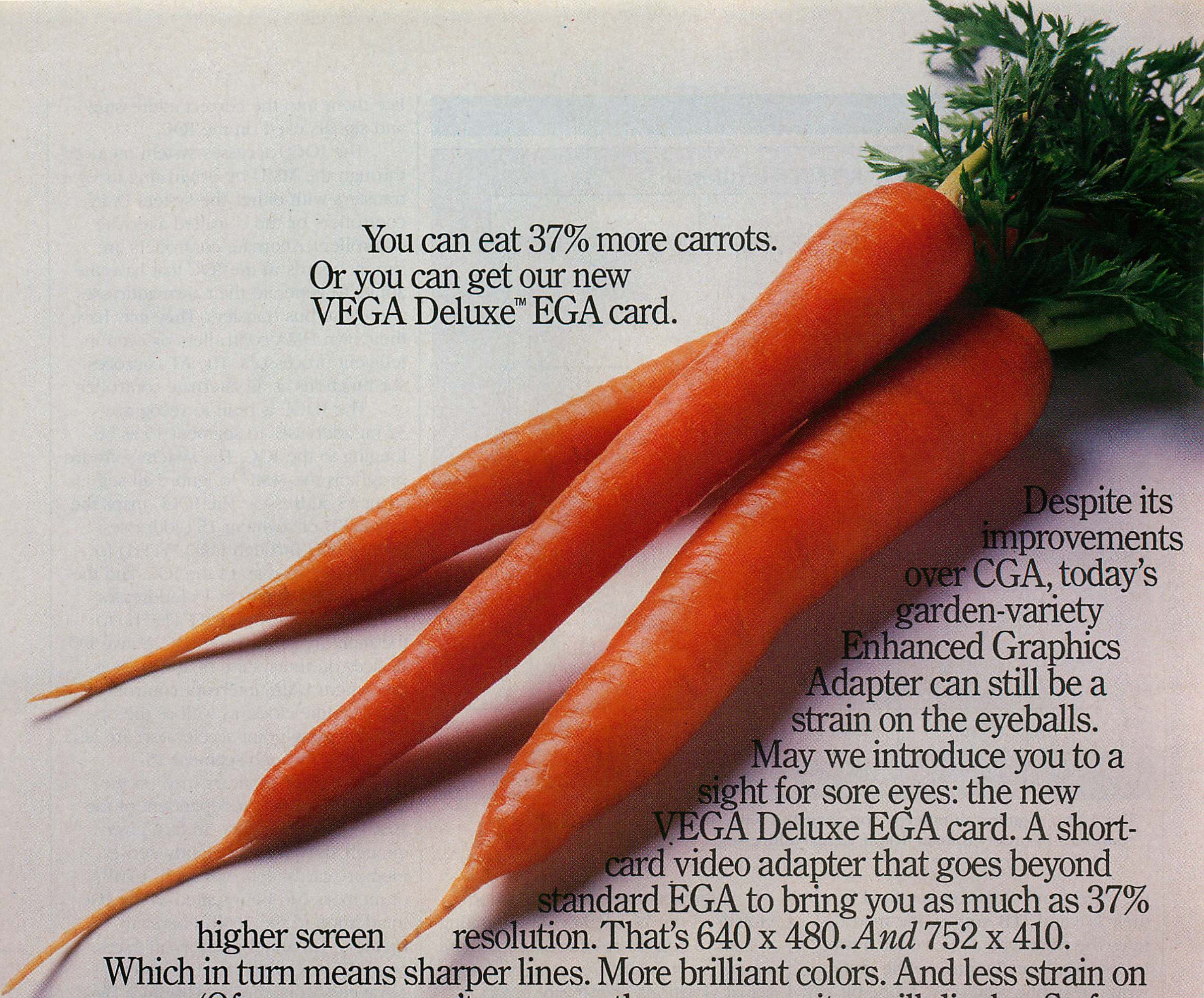

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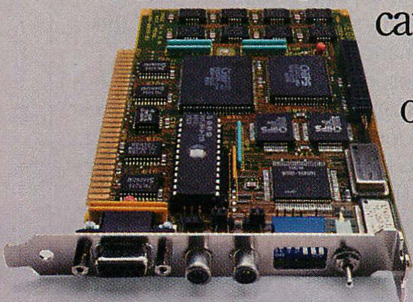

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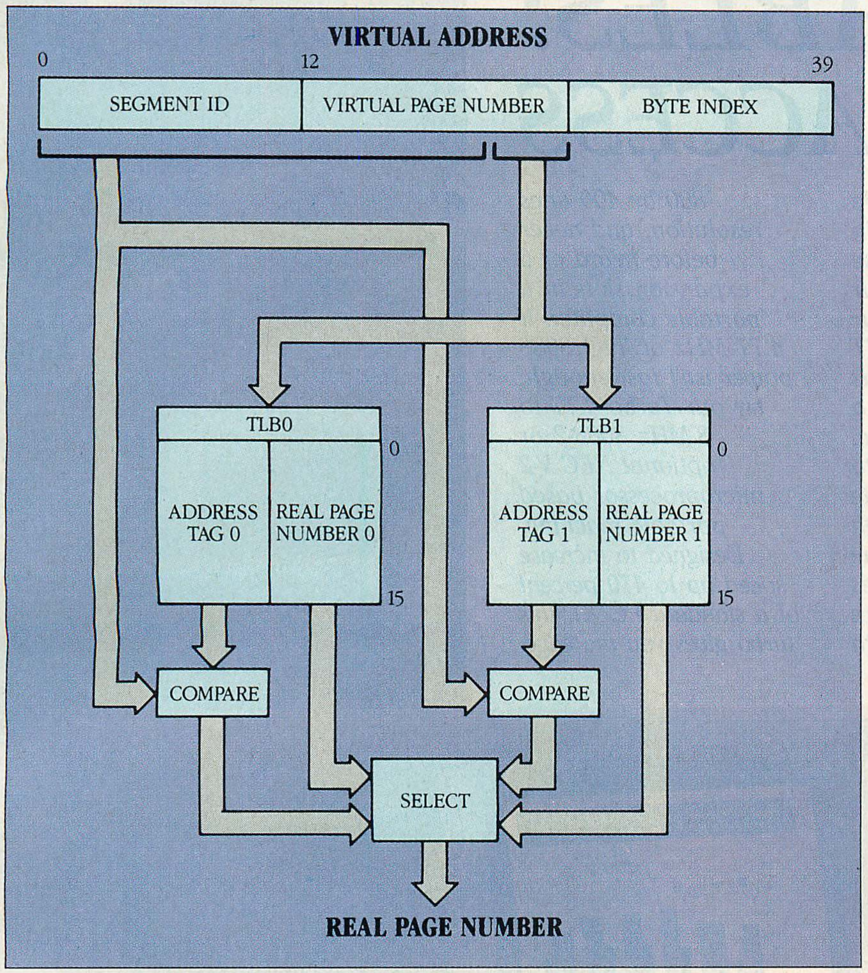
FIGURE 4: *Translation Look-aside Buffer*



Adapted from IBM RT PC Hardware Technical Reference

The MMU contains two 16-entry translation look-aside buffers (TLBs), which are indexed in parallel by the low-order four bits of the virtual page number.

called the translation control word (TCW). The TCW operates in a way similar to the segment registers in the MMU. Address translation operates either in page mode, supporting 2,048-byte pages, or in region mode, with 32,768-byte regions.

The TCW contains two control bits: one indicates whether the resulting address is to be treated as real or virtual; the other selects either IOC or system memory as the target of the transfer. If the target is system memory, the transfer is passed to the MMU. In virtual mode, the upper byte is always E0H, forcing all IOC-originated memory accesses to segment 14, which can be mapped by the operating system as necessary. If the target is the IOC, then the IOCC performs the transfer immediately, without involving the MMU.

ARCHITECTURAL PLANS

Good architecture provides a construction plan for the present as well as a growth plan for the future. The RT architecture clearly meets both of these criteria. The current implementations of the RT offer system capabilities well beyond those of the traditional PCs, the most important being the provision of an extremely large, uniformly addressable virtual memory. The 64KB addressing limits of present PC architectures, even as mitigated by multiple segments, exact a real price in software complexity and system performance.

Direct hardware support for virtual memory management and protection, combined with a generous 16MB real memory capacity, make possible the safe and efficient implementation of multiuser systems. The current MMU chip is limited to addressing 16MB of real memory, but the architecture supports multiple MMUs. Future systems could support much more memory.

The physical I/O channel of the RT copies the standard 8- and 16-bit AT I/O channel, with some performance improvements, allowing use of a wide variety of adapters. The I/O channel is, however, the one part of the RT architecture that could be changed without seriously affecting users' software investments. Future RTs could have a full 32-bit I/O channel that accommodates physically larger boards and provides minicomputer-class peripheral support and system performance.

While not without important benefits, the unique proprietary processor is certainly the riskiest part of the RT architecture. The architectural advantages of a high-performance, pipelined processor with a large linear address space are clear, but must be considered relative to the overall system. Actual system performance, as IBM is continually reminding us, depends on many factors: among them are compiler efficiency, memory, and I/O usage. Users are insulated from hardware by software; it is the combined performance of the two that really matters.

Developers of new systems or those porting programs from other UNIX or C language environments should appreciate the features in the AIX operating system and the VRM real-time environment that make the RT system easy to set up, administer, and use. The RT is not a multiuser PC in that it does not directly run multiple DOS object programs. Systems based on the Intel 80386 are the only ones that offer the distant promise of integrating new 32-bit applications and existing PC object code in the same multiuser system. The AT coprocessor offers a solution for single-user operation of existing PC programs, but at a higher price.

The effect of PC-compatibility issues on the acceptance of the RT remains to be seen. If PC compatibility were free, then, of course, everyone would want it. But it is not free. The 80386 achieves PC compatibility by having an architecture remarkably similar to that of the 8086/80286, with extensions for 32-bit operation, and that is both good news and bad news. The compatibility is good if it is desired; the more complex architecture is a hotly debated liability/asset.

The marketplace will ultimately decide the importance of integrated PC compatibility in high-performance workstations. Meanwhile, the RT PC is the first arrival in the next generation of desktop virtual memory systems, and there are certainly more coming soon to a dealer near you.

Thomas V. Hoffmann, a consulting editor for PC Tech Journal, *is manager of systems development at RoadNet Technologies, Inc., located in Baltimore, Maryland.*

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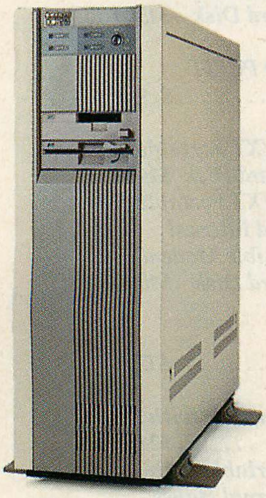

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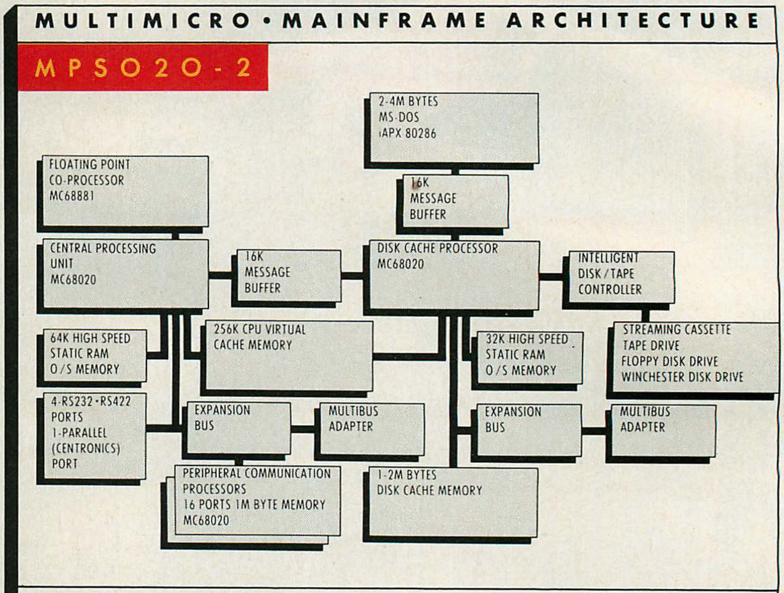

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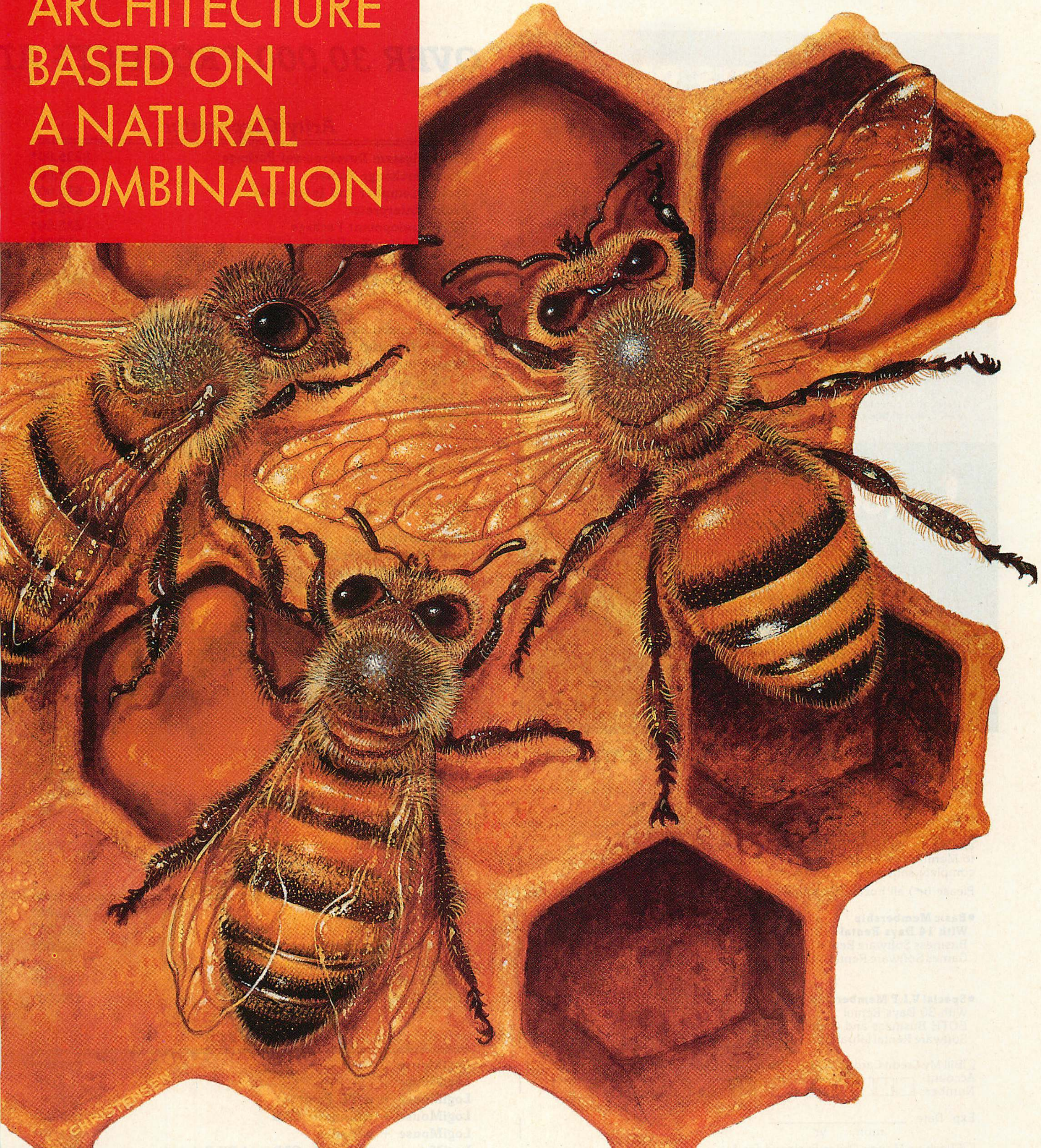

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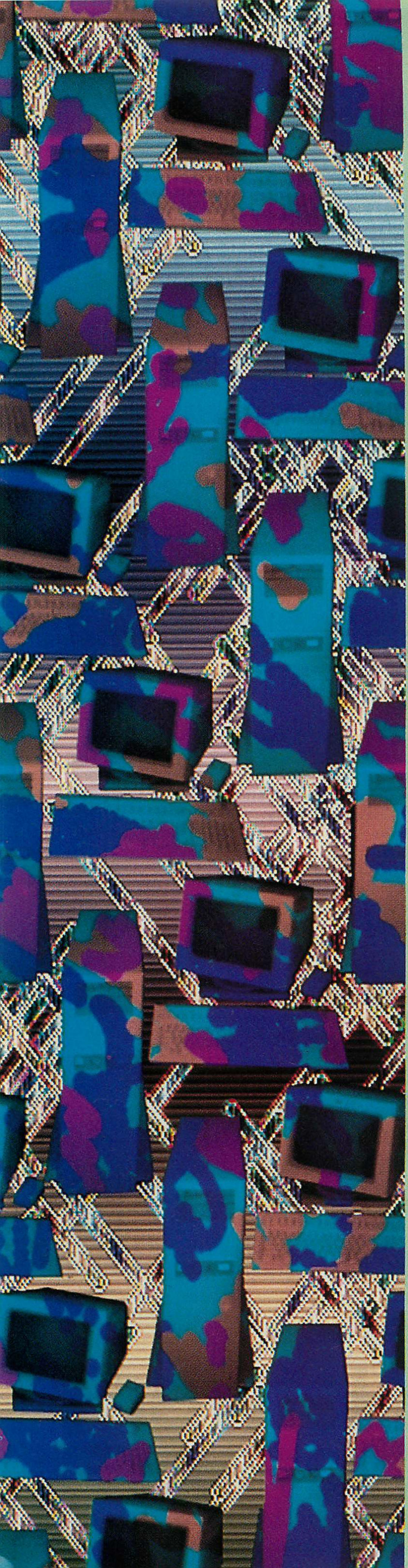

A progressive move by IBM, the Virtual Resource Manager is a layer of high-function software between operating systems such as AIX and the underlying RT PC hardware.

The Insulating Layer

RICHARD M. FOARD

The most significant architectural choice made in the RT PC software effort was IBM's decision to wrap a layer of high-function software around the RT's RISC processor and its I/O devices. This layer, the Virtual Resource Manager (VRM), is as much a part of the RT as BIOS is a part of 8086-based PCs, even though it is not delivered in ROMs inside the processor box. Like BIOS, VRM provides a more convenient software interface to system devices than is offered at the raw hardware level, but VRM contains far more than just a collection of subroutines and interrupt handlers. VRM is a complete realtime, multiprogramming operating environment and virtual memory manager as well as an I/O subsystem.

Although it was developed in close conjunction with IBM's adaptation of AIX (Advanced Interactive Executive) for the RT, VRM is not logically a part of AIX and does not depend on AIX in any way. Other operating systems can be adapted to run atop VRM, or realtime application systems can be built to run directly on VRM, without any mediating services from an operating system.

Some similarities are apparent between the VRM and IBM's venerable VM/370. Both can support the concurrent operation of several operating systems on a single machine. Unlike VM/370, however, VRM implements a very high-level virtual machine that has never been and likely never will be implemented in hardware. VRM meets the

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software it hosts in a well-defined interface called the Virtual Machine Interface (VMI), see figure 1. On the RT, I/O control and processor allocation functions embodied in conventional operating systems have been "pushed across" the interface into the VRM.

As shown in figure 2, it is the VRM that issues real physical I/O instructions to devices and receives real hardware interrupts back. Operating systems such as AIX use VRM as an intelligent middleman in dealing with I/O devices, and consequently see ***virtual*** devices and ***virtual*** interrupts. From an AIX system programmer's viewpoint, virtual devices have several desirable attributes not shared by their real counterparts. For one thing, they are very intelligent—each one can be viewed as having an RT built into it; they can accept and process very high-level commands. For another, it is not necessary to replicate hardware to replicate virtual devices: one physical terminal, for example, can serve as many virtual terminals.

Sandwiching VRM's intelligence between the RT processor and its hosted operating systems allowed IBM developers to meet the four design goals that guided the RT software development effort, as set forth in *IBM RT Personal Computer Technology* (IBM, 1986):

- To provide a high-level machine interface that simplifies the development and implementation of operating systems and their applications.
- To maximize performance in order to provide support for realtime, process-control-type applications.
- To provide an extendable, flexible interface that allows users to customize the system to meet their needs.
- To provide compatibility with IBM PC applications by supporting an Intel 80286 coprocessor.

USING VRM FACILITIES

In traditional computing environments, the operating system lies at the lowest level of system software and performs direct control of the processor and its I/O device hardware. Operating systems under VRM on the RT are different—they are one level removed from the physical hardware. Their device drivers do not execute direct hardware control instructions. Instead, they serve as high-level routers of commands and data. Where the traditional operating system disk driver issues seek and read instructions directly to a disk controller, its RT counterpart issues VRM supervisor calls (SVCs). The SVCs are hardware instructions to a ***virtual*** machine. Like the traditional driver, the RT driver receives completion interrupts, but the interrupts are virtual ones caused by VRM software instead of real ones caused by disk controller hardware.

The VMI is made up of this set of supervisor calls, along with the virtual interrupts and environmental conventions that the VRM provides to the software it hosts. The virtual machines implemented by VRM are versatile ones that provide operating systems such as AIX with execution control, memory management, I/O service, and communications with other virtual machines.

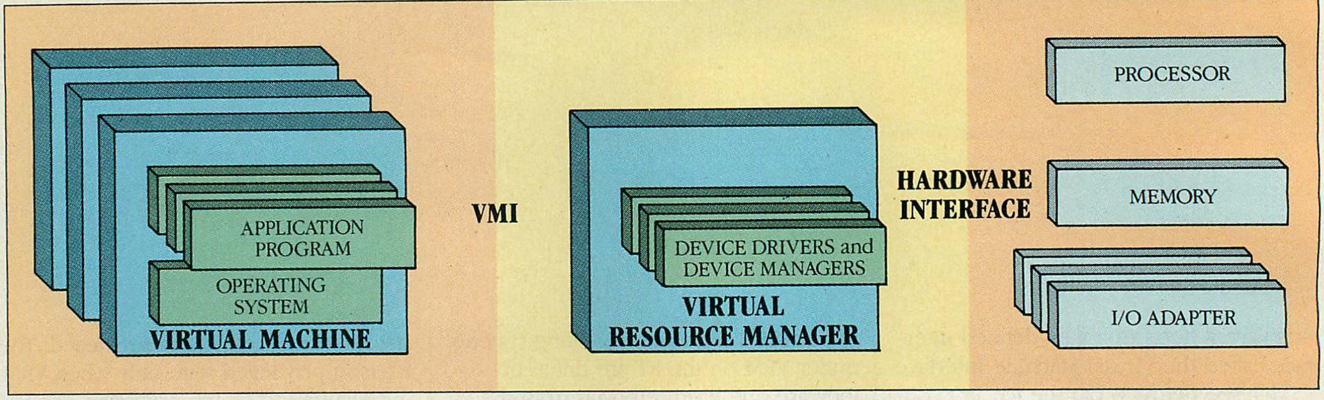
VRM's SVCs are accomplished using the RT's SVC instruction, which includes a 16-bit function code. This instruction serves many purposes in a typical RT software environment. It is used for calls from application to operating system, from operating system to VRM, and from VRM to VRM. SVCs with function codes 0 through 32767 are pass-through SVCs. Functions greater than 32767 are reserved for calls to VRM. All SVCs cause VRM's SVC handler to gain control; but, pass-through SVCs are immediately routed back up to an operating system executing in a virtual machine after a quick legality check (see figure 3). AIX SVCs made from an application program, for example, are received and immediately forwarded back up to the AIX virtual machine, where the AIX kernel processes them.

VRM performs limited legality checks on SVCs using a simple scheme based on two kinds of RT execution states—privileged and unprivileged. The RT is in privileged state only when VRM is executing to switch processes or service I/O. In the unprivileged state, programs are prevented from executing instructions that exert direct control over the hardware operating environment. While it is executing in either an operating system or application program (problem state), VRM is running a virtual machine, and executes in the processor's unprivileged state.

An operating system such as AIX running as a VRM virtual machine can call on VRM for a number of execution control services. By making VRM SVCs, it can enable or disable virtual interrupts on seven levels, initiate a software interrupt, or return from a virtual interrupt service routine. Other SVCs allow the operating system to give control to an application program (switching from operating system to problem state), or to receive control back from a terminating application program (switching from problem to operating system state). An operating system can call on VRM to cause its entire virtual machine to idle, waiting for a virtual interrupt to occur. While one virtual machine idles, VRM allows others to run. An operating system can shut itself down entirely, by calling on VRM to terminate and destroy its virtual machine.

Using the VRM memory management services, a virtual machine can exercise low-level control over the allocation and use of real and virtual memory. Each virtual machine can create, change, copy, or destroy memory segments. The Map Page Range SVC allows an operating system to establish a mapping between a range of pages in a segment and a set of blocks on a disk. Because the blocks need not be contiguous on the disk, an operating system can use this call to "window" an entire file into the virtual address space and take advantage of the RT's memory management capabilities to address the contents of the file as if it had been read into a memory array.

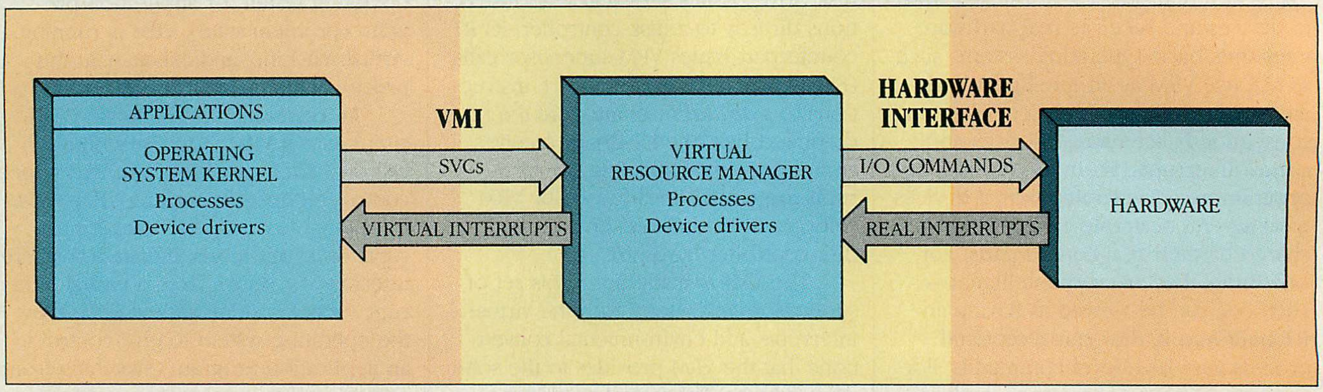
FIGURE 1: *RT PC Software Design*



The VRM meets the software it hosts in a well-defined interface termed the Virtual Machine Interface, which consists of supervisor calls (hardware instructions to virtual machines), virtual interrupts, and environmental conventions for hosted software.

Adapted from IBM RT Personal Computer Technology

FIGURE 2: *RT PC System Structure*



Operating systems such as AIX use the VRM as an intelligent middleman in dealing with I/O devices and receiving interrupts.

Adapted from IBM VRM Technical Reference

Pin Page Range ensures that no page fault will be encountered when reading or writing a specified range of virtual addresses. Operating systems and their hosted application programs can ensure that performance-critical data structures remain quickly accessible by loading and "pinning" regions of memory. Other SVCs provide control over page-wise memory protection attributes, and allow the explicit purging of virtual pages from fast memory when they are no longer required.

VRM's I/O SVCs allow hosted operating systems, each running in its own virtual machine, to operate and share the RT's peripheral devices. Each device under VRM's management, whether a real or virtual device (such as a virtual terminal), is identified by a unique I/O device number (IODN). Within the 65,536 possible 16-bit IODNs, VRM enforces the following conventions: IODNs 1 through 1023 are reserved for devices defined at initial program load (IPL); 16384 through 32767 are reserved for minidisks; 32768 through 65535 identify virtual devices (logical devices of which many instances may share one physical device).

VRM device management services are available to hosted operating systems on a flexible, dynamic-attachment basis. Virtual machines that want to establish access to a particular device call on VRM by passing an IODN. VRM makes up a connection, or *path*, to the device, and returns a path identifier that is used by the virtual machine to conduct its business with the device.

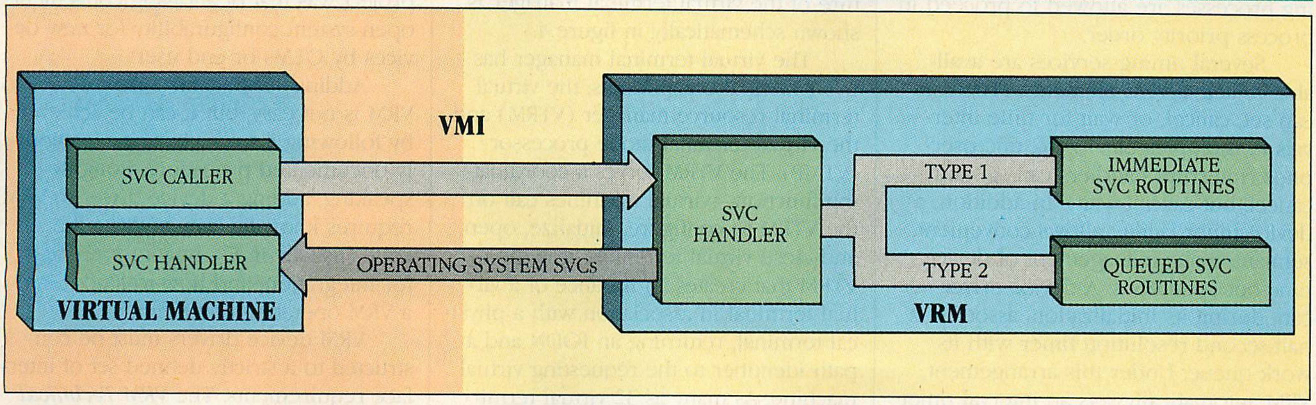
Many VRM SVCs support I/O device attachment, data transfer, control, and detachment. Using the Query Device SVC, a virtual machine can learn which IODNs are currently defined within VRM and the characteristics of their associated devices. Once it has identified the devices it requires, a virtual machine executes Attach Device SVCs to establish logical pathways. Given pathways, the machine is free to use VRM's Send Command and Start I/O SVCs to conduct synchronous or asynchronous I/O operations on its attached devices.

A device need not be dedicated for the exclusive use of a single virtual machine. Devices that can support shared use can be "attached" and used by multiple virtual machines simultaneously. Under VRM control, I/O devices are treated as a resource pool for which concurrently running virtual machines contend, and then share.

Virtual machines can add device management capabilities to VRM using the Define Code and Define Device SVCs. Define Code takes an executable module as a parameter, loads it into memory, and, in effect, dynamically links it into VRM. Define Device assigns an IODN to a device and informs VRM of the device's characteristics. Together, these two SVCs can graft new device drivers into VRM without stopping and restarting a running system.

VRM's I/O SVCs allow virtual machines to exchange messages, permitting intermachine coordination, resource sharing, and notification of exceptional conditions. VRM also provides a family of SVCs for machine con-

FIGURE 3: *SVC Types*



Adapted from IBM VRM Technical Reference

The VRM supervisor call handler routes calls from application to operating system, from operating system to VRM, and from VRM to VRM. The VRM performs limited legality checks on SVCs using a simple scheme based on the RT's execution states.

trol. Using VRM calls, a virtual machine can terminate its own operation, cause the booting (IPL) of another machine, call for the IPL of VRM itself, request information about all currently running virtual machines, or learn the physical processor's hardware serial number. A Debug Virtual Machine SVC permits the flagging of a particular virtual machine to cause automatic invocation of the debugger the next time it is given control of the processor.

VRM INNER WORKINGS

Within VRM lies a flexible, realtime multiprogramming operating environment with special extensions that allow it to present the illusion of several virtual machines running concurrently and independently on a single processor. VRM consists of processes, device drivers, and device managers.

VRM processes are functionally identical to those of higher-level operating systems, such as UNIX; they are asynchronously executing paths of instructions that can run concurrently with each other and with interrupt service procedures. VRM device drivers are likewise analogous to their counterparts in conventional operating systems; they are made up of one or more subroutines that can be called from applications, and they usually operate in concert with interrupt service routines.

Device managers provide support for devices too complex to be serviced under the simple device driver arrangement. Device managers implement virtual terminals, for example, allowing a single physical terminal device to be simultaneously connected to and switchable among many different application programs or even among different virtual machines. Along with SVC handlers that route and queue I/O requests and virtual interrupts, VRM device drivers and device managers make up the VRM I/O subsystem.

In IBM's off-the-shelf AIX environment, the VRM system presents a single virtual machine to higher-level software; the single machine is dedicated to serving AIX requirements. Although several VRM processes participate in the AIX/VRM environment, one special process is responsible for coordinating all VRM activities in providing this virtual machine. This process, along with its data structures and state information, *is* the AIX virtual machine. In environments where many virtual machines run concurrently and compete for hardware resources, one controlling VRM process exists for each machine. When VRM switches control of the processor from one virtual machine's process to another, the effect is to deactivate one virtual machine and activate another.

Processes and interrupt handlers are the active elements in a VRM-based system. They operate on each other and on queues, semaphores, paths, devices, and modules. Devices and modules carry 16-bit logical names; each device is assigned an IODN and each module carries an IOCN (I/O code number).

Within a running VRM system, each system element is referenced by a 32-bit identifier (even devices and modules already carrying IODNs and IOCNs are assigned identifiers). In addition to distinguishing system elements, the 32-bit identifiers contain an encoding of the element's type, generation, and an index with which to locate its associated element control block quickly. These identifiers are assigned dynamically by the system, as VRM initializes and as elements are created during the course of normal processing. VRM uses the embedded type and generation data to apply validity checks to ensure that only sensible operations are applied to system elements.

VRM processes contend for processor time on a simple priority basis, under the control of VRM's scheduler, or *process dispatcher*. Execution priorities range from 0 (the highest) to 15. The dispatcher implements a preemptive scheduling discipline under which processes of higher priority than the one currently running are given immediate control if they become ready. The dispatcher also can accommodate round-robin sharing for processes at the same priority level.

The internal VRM environment provides processes with a host of runtime services. Most, such as interprocess message queuing primitives, synchronizing semaphores, and a debugger, are general-purpose facilities of the sort found in most realtime systems.

VRM processes and device drivers communicate messages and work requests among themselves with VRM's queuing mechanism. Each device has an associated queue. When a virtual machine process makes a Start I/O SVC to VRM, VRM uses the queuing facility to enqueue a request to the appropriate device driver. In addition to calls for enqueuing, dequeuing, and inspecting queue elements, VRM provides for the dynamic creation and destruction of queues and for the establishment of logical, synchronized data pathways between communicating VRM elements.

The semaphores are prioritied extensions of standard Dijkstra synchronizers. Each semaphore has an associated resource count. If the count is positive, a process attempting to receive a unit of resource from the semaphore is allowed to consume the unit and proceed; if it is 0, the process waits. When

other processes free resource units by sending them to the semaphore, attending processes are allowed to proceed in process priority order.

Several timing services are available to active VRM elements. Processes can set, cancel, or wait for time intervals in multiples of 975.562 microseconds (interrupt handlers can set and cancel, but cannot wait). In addition, a device timer facility allows convenient, semiautomatic management of device time-out conditions. A device driver can, during its initialization, associate a half-second resolution timer with its work queue. Under this arrangement, VRM automatically sets an interval timer each time the I/O initiate-entry point of the driver is called, and cancels the timer when the request is dequeued following its timely processing.

STANDARD DEVICE MANAGERS

In its standard configuration, the VRM I/O subsystem includes two key, high-function device managers, one for minidisks and one for virtual terminals.

Minidisks. The minidisk manager enables VRM-hosted software to partition physical disk storage into subareas that can be managed independently. A minidisk is a contiguous area of disk storage on a single drive. In a typical AIX environment, one minidisk is devoted to VRM and its associated device driver files, one is reserved as a paging area for use in virtual memory management, and several more hold AIX file systems that can be grafted into the hierarchical AIX directory structure.

(Because of the vastness of the RT's terabyte virtual address space, it is not feasible to allocate a paging minidisk large enough to accommodate the largest possible loading of memory. System managers therefore must select a paging minidisk size by estimating the largest expected memory loading. The RT's memory management code will terminate system operation if the capacity of the paging minidisk is exceeded.)

VRM virtual machines can dynamically control the allocation of disk space among minidisks. Operating systems such as AIX, which offer a high degree of flexibility in managing disk storage, pass direct control of minidisk allocation to the system user. The AIX **minidisks** command allows a system manager to perform minidisk control functions directly from user command level.

Virtual terminals. The VRM virtual terminal manager provides control of a set of physical terminals and their associated devices, creates virtual terminal abstractions atop physical terminals, and manages data traffic among VRM virtual machines and virtual terminals. The structure of the virtual terminal manager is shown schematically in figure 4.

The virtual terminal manager has two principal components: the virtual terminal resource manager (VTRM) and the virtual terminal mode processor (VTMP). The VTRM serves a coordinating function—virtual machines call on the VTRM to configure, initialize, open, and close virtual terminals. It is the VTRM that creates an instance of a virtual terminal in association with a physical terminal, returning an IODN and a path identifier to the requesting virtual machine. As many as 32 virtual terminals may be simultaneously associated with each physical terminal device.

Once a virtual machine has created an instance of a virtual terminal, it uses the VTMP services to communicate with it. The VTMP provides a model of one logical terminal for each active virtual terminal. By default, the VTMP provides the virtual terminal user program with terminal interaction in keyboard send/receive (KSR) mode. In KSR mode, the virtual terminal emulates an ASCII terminal recognizing ANSI 3.64 controls. The alternate, monitored mode (MOM), provides a more direct path from user program to display hardware and a shortened input path for keyboard and locator (mouse) input.

Adding support for a device to VRM, while not easy, is achieved by following a well-conceived, copiously documented procedure.

In either mode, the VTMP provides the program with information about available fonts and colors and permits control of terminal devices such as keyboard lamps and speakers. The VTMP also allows the setting of locator horizontal and vertical movement thresholds and accepts specification of locator movement scaling factors.

ADDING DEVICE DRIVERS

In its standard configuration, the VRM/AIX software environment includes the minidisk manager, the virtual terminal resource manager, and driver support for asynchronous serial ports, diskette drives, hard-disk drives, parallel ports, and a streaming tape drive. High on IBM's list of software goals in the RT project was that of allowing convenient open-system configurability for new devices by OEMs or end users.

Adding support for a new device to VRM is not easy, but it can be achieved by following a well-conceived, copiously documented procedure. Roughly speaking, adding a device driver to VRM requires knowing how to write the code (usually in C), how to prepare it for integration, and how to load it into a VRM operating environment.

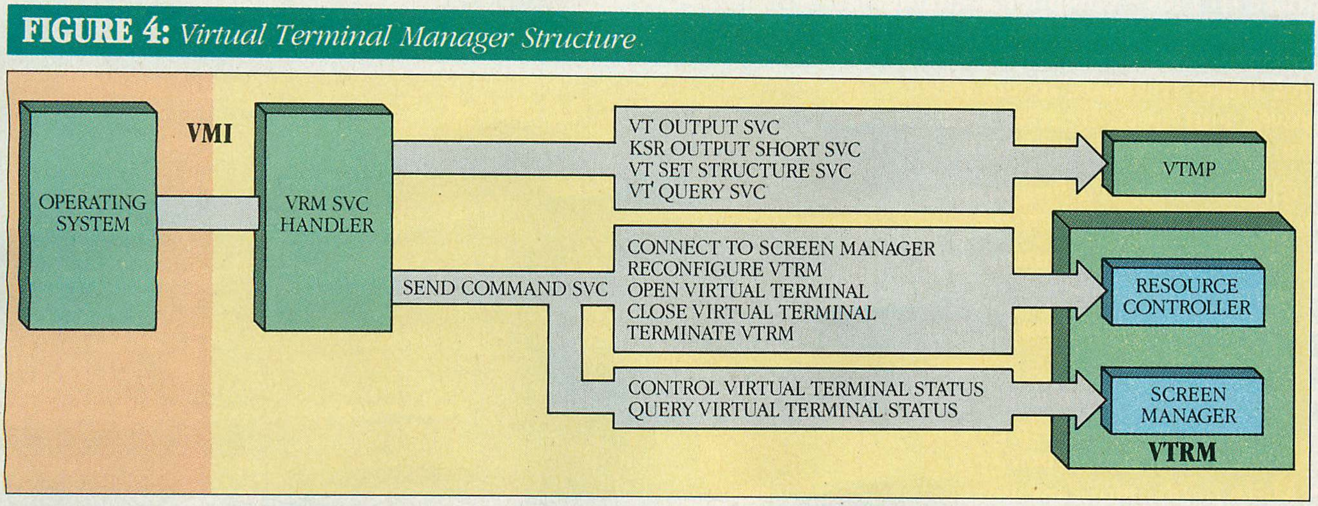
VRM device drivers must be constructed to a strictly defined set of interface requirements. The *VRM Technical Reference Manual* delineates the context in which drivers run and the set of functions they must perform. Each of the drivers is constructed as an executable module with a single entry point; all services for which the surrounding environment must rely on the driver are obtained by calling its single entry point with a function code, a data area, and the length of the data area. The interpretation of the data area's contents depends upon the function invoked.

Figure 5 illustrates the functions a driver must provide to VRM. The first call a driver must handle is the invocation of its device definition function. VRM first calls on a device driver when it receives a Define Device SVC from a virtual machine. At definition time, a driver is passed the address of a define device structure (DDS)—a data structure containing details of the device's hardware characteristics, such as its I/O port addresses and DMA type, error-logging information, and other operating parameters controlling how the driver may be called.

VRM invokes a device's initialization function each time it receives an Attach Device SVC for the device. The driver performs this function by allocating all the queues, control blocks, and other resources required to operate the device, and by sending the necessary hardware instructions to make the device ready for use. It thus enables its interrupt level and DMA channel.

A device's termination is the opposite of its initialization. A driver is called to perform termination when VRM receives a Detach Device SVC. It terminates by completing pending I/O operations, releasing resources held in conjunction with the device, and performing any other necessary tasks.

The VRM drivers' ability to support initialize (attach) and terminate (detach) functions allows the system to be both frugal and flexible in its management of



Adapted from IBM VRM Technical Reference

Among other duties, the virtual terminal manager handles data traffic between VRM virtual machines and virtual terminals.

resources even under highly dynamic work loads. Because detaching a device releases its associated resources, they are not engaged when idle and are available to be used elsewhere. The ability to attach and detach dynamically also allows the serial sharing of devices that cannot be used concurrently by multiple virtual machines.

A typical driver's most frequent interaction with the environment comes in the form of calls to its I/O initiation and interrupt-handling functions. Its I/O initiation function is invoked as the result of VRM receiving a Send Command or Start I/O SVC. VRM conveys these requests to a device driver by depositing 32-byte messages in the driver's input work queue, then invoking its I/O initiation function once for each message in the queue. More precisely, VRM first calls on the device's **check parameters** function to validate an I/O request, then enqueues it if the parameter checker approves its contents. A device's processing of a call for I/O initiation typically involves starting a hardware operation and noting status information for reference later, during the processing of a completion interrupt.

A driver must provide a device-specific interrupt-handling function to VRM in the form of a second-level interrupt handler (SLIH). Because interrupt levels can be shared by multiple devices, each level also has an associated first-level interrupt handler (FLIH); a level's FLIH determines which of several devices on a level is interrupting by calling all the level's SLIHs in succession until one determines that its own device of interest is interrupting. The SLIH then consumes the interrupt, performs whatever device processing is necessary to complete the I/O operation, and dequeues the work queue element that commissioned the operation. Dequeuing the work request causes VRM automatically to generate a 32-byte acknowledgement message and queue it back to the system element that requested the operation (detailed status information for the message is provided by the driver). If a virtual machine requested the operation, it receives the acknowledgement by means of a virtual interrupt.

In addition to standard interrupt processing, VRM supports off-level interrupt processing. In high-performance, time-critical I/O situations such as the servicing of high-speed asynchronous communications lines, SLIH designers have the option of performing partial, minimal processing when an interrupt is first received, then deferring further processing until interrupt activity has subsided. VRM makes note of deferred interrupt processing work in a scheduled off-level interrupt processing queue and delivers it back to the driver for completion later.

Device driver program modules must be built in conformation with a set of general coding requirements. IBM provides assembly and C language development tools for VRM that run under AIX. A device driver, regardless of the language in which it is coded, must support the C subroutine linkage scheme, be memory location-independent, and, oddly, may contain no more than one reference to any given external name. (Driver architects, consequently, must funnel multiple calls to external subroutines through a local interface subroutine.)

Driver developers also have the VRM Debugger, which can execute with just the VRM nucleus and a PC monochrome display or a standard terminal and a serial adapter. The debugger can be given control when the system terminates abnormally, when a preset breakpoint is executed, or when a special keyboard sequence is entered. Alternatively, a VRM supervisor call allows the debugger to gain control automatically when a user-designated virtual machine is dispatched to run.

A developer who has created a new VRM device driver must choose one of three methods for configuring the device into the VRM system: install it on the VRM minidisk for automatic loading at VRM IPL time; tailor AIX configuration files to cause AIX to load the driver as part of AIX initialization; or construct the AIX application to call directly for its definition, loading, and attachment. (If the device is to be used from AIX, the developer also may need to generate a simple AIX-level driver into the AIX kernel to provide access to the VRM driver.)

VRM AS REALTIME SYSTEM

Although VRM is viewed as a supporting player to AIX, developers undoubtedly will exploit its capabilities as a realtime operating system in its own right. VRM facilities for process management, interprocess synchronization and communication, memory management, and synchronous or asynchronous I/O make it a match for any stand-alone commercial realtime system. Its dynamic configuration abilities, in fact, are not found in most commercial systems on micro- or minicomputer-class machines.

The fact that VRM coexists symbiotically with AIX raises interesting possibilities for hybrid systems in which conventional application programs run normally as AIX programs, while realtime application processing is under control of another VRM virtual machine and its cooperating processes. VRM's preemptive scheduling discipline can be used

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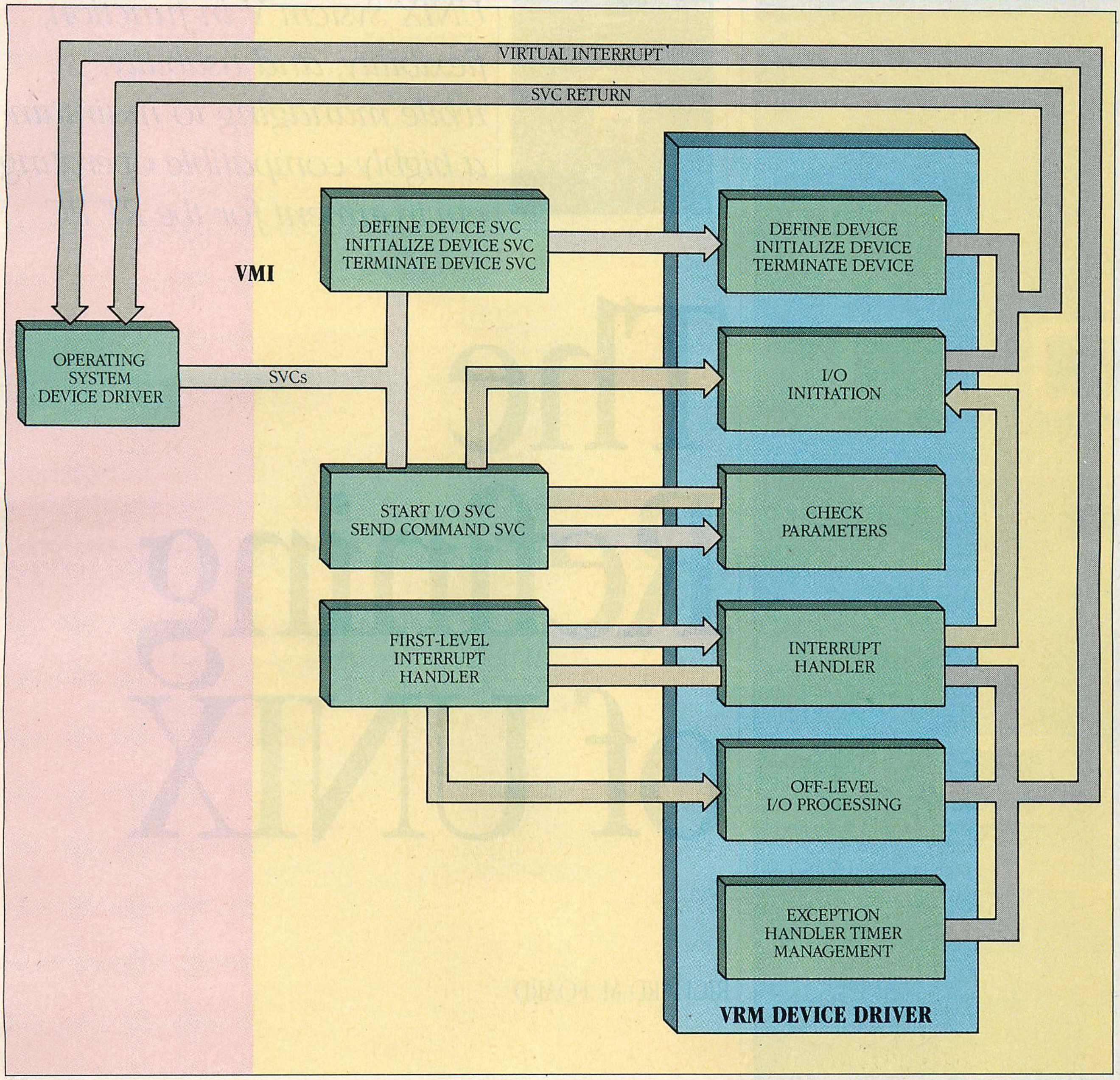
FIGURE 5: *VRM Device Driver Functions*



Adapted from IBM VRM Technical Reference

Device drivers perform a strictly defined set of functions. Each driver is an executable module with a single entry point.

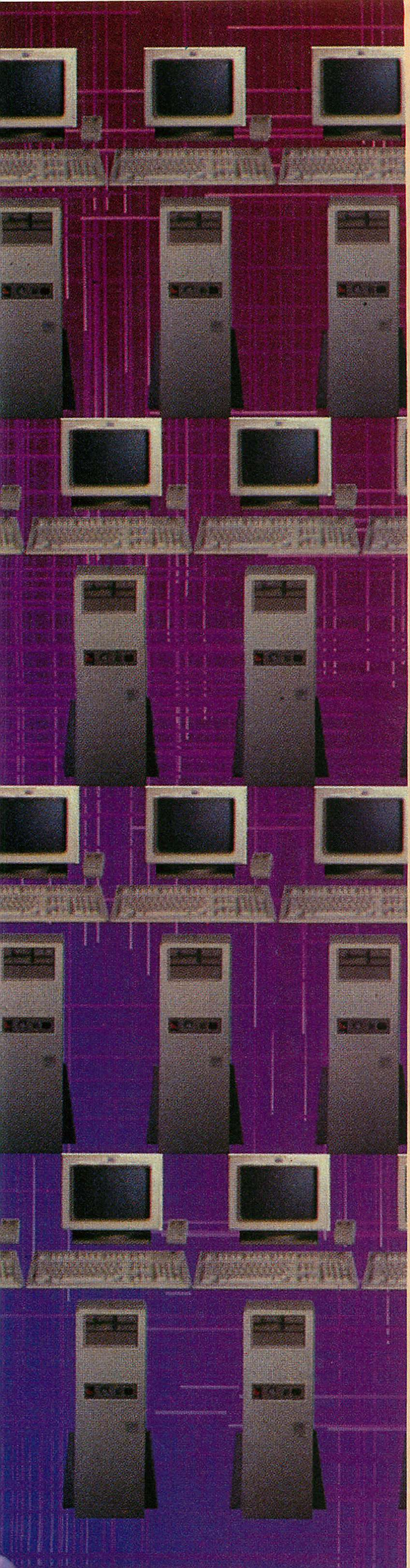
to ensure that time-critical realtime processes take precedence over AIX virtual machine support processes.

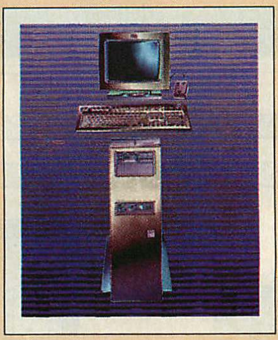
Developers of VRM-based applications do not have to go far to find a cross-development environment. AIX provides all the compiling, linking, and configuration tools required to develop VRM code. Except for the odd restriction that VRM modules may have no more than one reference to each external symbol, VRM coding conventions are easily met using C or assembly language under AIX.

With the inclusion of VRM in the system, the RT PC can be viewed as coming with built-in, operating system-independent device drivers. By dramatically reducing the amount of work required for third-party software developers to erect systems-level software on the new ROMP processor, IBM has made the RT a much more attractive commercial platform. Along with the widespread use of high-level languages such as C, VRM goes a long way toward eliminating the obstacles to software migration that are usually posed by new machine architectures.

To software architects and IBM watchers, VRM is at worst an interesting experiment and at best a model approach to harnessing the growing power and taming the increasing complexity of workstation-level computers. To software providers, it is a flexible, high-performance, realtime environment and a vehicle for providing painless integration of support for new devices into AIX. To operators and end users of AIX systems, it is a barely visible, but powerful extension, to the native capabilities of AIX and the RT PC.

Richard M. Foard, a consulting editor for PC Tech Journal, *is manager of product development at RoadNet Technologies, Inc., located in Baltimore, Maryland.*





With AIX, IBM has surpassed UNIX System V in function, flexibility, and usability, while managing to maintain a highly compatible operating environment for the RT PC.

The Refining of UNIX

RICHARD M. FOARD

In assembling the RT PC software environment, IBM took on an extraordinary number of challenges at one time. With the Advanced Interactive Executive (AIX), it stepped squarely into the UNIX System V business. The RT's novel, soft virtual machine architecture makes configuration for new devices a painless process; in many cases it does not even require regenerating the AIX kernel. IBM forged an elegant arrangement that allows application programs to take full advantage of the RT's revolutionary memory management agility. It shored up weaknesses inside the UNIX kernel. It introduced "virtual devices." It built an optional data management layer on top of UNIX's well-conceived but rudimentary file system. It unleashed yet another UNIX text editor on the world. Finally, it improved UNIX's legendary user-unfriendliness, or at least made a creditable try.

IBM is, as always, coy about the size and scope of its software tooling effort, but compared to most UNIX ports, the task must have been staggering. That IBM chose UNIX System V as the base from which to build AIX is not news. UNIX is entrenched as the operating system of choice in the engineering/scientific workstation marketplace. What *is* news is the thorough attack that AIX developers mounted on UNIX's time-honored deficiencies. Their efforts have produced an operating system that far surpasses UNIX in function, flexibility, and usability, yet provides a highly com-

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patible target for porting existing UNIX applications and knowledge.

In repairing UNIX shortcomings, AIX developers made sweeping enhancements below, within, and above the UNIX kernel. Layered below the kernel, between AIX and the RT's I/O and memory management devices, is the Virtual Resource Manager (VRM), a realtime execution environment that directly controls the RT's hardware while presenting a uniform, high-level interface to the AIX kernel.

Within the kernel, UNIX's standard interprocess signaling facilities have been augmented by newly engineered shared memory and signal management primitives. In cooperation with VRM, the AIX kernel supports the RT's virtual memory architecture, allows highly dynamic configuration for I/O devices, and incorporates advanced error-logging mechanisms.

Lying atop the kernel, right next to UNIX's standard Bourne and C shell user-interface programs, is the Usability Services layer, which gives the user the ability to invoke and control programs in a menu/mouse/pop-up window environment instead of in UNIX's terse, arcane, native tongue.

AIX-based applications can call on UNIX's standard, low-level, flat, file management system, or they can use a set of optional extended file and data management facilities; these include a B-tree indexed access method, relational data modeling tools, and a Structured Query Language (SQL) interface. AIX applications also have the option of calling on the RT's unique virtual memory capabilities to map DASD (direct access storage device) resident program and data files directly into the virtual address space. This feature provides a single-level storage capability like the one introduced in IBM's System/38.

The litany of the AIX environment's extensions to standard UNIX is quite long. If the RT were just another UNIX machine, there would not be much to say about it, at least not to the UNIX initiates. This article focuses more on how AIX is different from UNIX rather than how it is the same.

TWO FEET OF SOFTWARE

The sheer bulk of the RT's standard software package is quite intimidating. Occupying two feet of shelf space, the packaged AIX software environment is a far cry from the current PC family's single DOS binder. Software developers who have ordered the optional AIX and VRM technical reference manuals or licensed program products such as *Applix* confront an even bulkier set of software and literature.

IBM offers some guidance in the form of a *Library Overview and Reading Sequence* brochure and a comprehensive *Bibliography and Master Index* volume. The brochure sketches the contents of the other documents and suggests a reading sequence. The master index provides the point of reference from which users can locate information in any of 24 standard and optional RT PC reference books.

One entire reference volume is dedicated to software installation. Its eight chapters lead the reader, in well-considered, painstaking detail, through the VRM and AIX software installation and configuration processes. Although the prospect of an eight-chapter installation process may seem intimidating, the software installation for a standard hardware set can be done quickly even by a (careful) first-time user.

System software comes on a set of eighteen 1.2MB diskettes, grouped into Installation/Maintenance, VRM, AIX Operating System, Usability Services, Multi-User Services, and Extended Services sets. The system installation requires booting and installing the VRM, then installing the "base system program" (AIX), and loading the desired sets of additional system programs.

During the installation process, the user gets a first look at some of the features that, from an operational viewpoint, distinguish AIX from other UNIX implementations. From the time the first VRM diskette is bootstrapped, the system walks the user through a menu-based dialogue in which decision points, and the consequences of taking the default choices, are clearly explained at each step. No prior experience with UNIX is required. For those users who in the past have been terrorized and misled by obscure UNIX installation procedures, this is by far the least anxiety-provoking of the lot. The menu-driven AIX installation procedure leads the user as far as the loading of the / (root) and /usr file systems along with their standard contents.

In normal operation as well as during installation, AIX, VRM, and their companion products can produce a vast array of error, exception, and information-only messages on the system console or the system unit's LED display. IBM has chosen a uniform, centralized approach to providing message explanations by cataloging all the messages the system is capable of producing in a single, massive *Messages Reference* volume. Organized by product name and numeric message class code, messages are listed with probable causes and suggested corrective actions. However, the messages themselves tend to be verbose and usually provide sufficient information for the user to solve problems without consulting the book.

After installing VRM, the user may choose to use the **devices** and **minidisks** commands to customize the system. **Devices** reports on the current operating system device driver configuration and allows the addition, deletion, or reconfiguration of system device drivers (see photo 1). **Minidisks** provides for the creation and destruction of VRM-maintained hard-disk partitions called *minidisks* (see photo 2).

Separate minidisks, each of which must be wholly contained on a single hard-disk drive, hold the VRM file system, a virtual memory paging area, the optional AT coprocessor's DOS file system, and AIX file systems. Minidisk-resi-

PHOTO 1: *Devices Command Screen*

```
The following devices are configured in your system.
A zero (0) in the Port, Slot, or IODN field indicates information is
not available or not applicable.

Name      Type      Class     Adapter                        Port Slot IODN

coproc    coproc    coproc    ** Description Not Available   0    0    2050
lp0       opp       printer   IBM Mono Disp & Paral Prntr    1    3    12000
hdisk0    hdisk0    disk      IBM RT PC Fixed Disk/Diskett   0    0    1
hdisk1    hdisk1    disk      IBM RT PC Fixed Disk/Diskett   0    0    2
hdisk2    hdisk2    disk      IBM RT PC Fixed Disk/Diskett   0    0    3
fd0       fd0       diskette  IBM RT PC Fixed Disk/Diskett   0    0    4

To RETURN to the list of commands, press Enter.
To PRINT this list of devices, press F4.

> _
```

The devices command reports on the current operating system device driver configuration and allows the addition, deletion, or reconfiguration of system device drivers.

PHOTO 2: *Minidisks Command Screen*

```
Fixed Disk hdisk0 has the following minidisks:

MD   MD    MD      Block Number MD     Mount                   Auto Auto  R/W
Name IODN  Type    Size  Blocks Locatn Directory               IPL  Mount Status

hd6  32760 VRM     512   2284   B      /vrm                    N    Y     R/O
hd4  16385         512   2400   B                              N
Available Space    512   19261  B      ****************************************
     32766 PgSpace 512   19436  B,M                            N
Available Space    512   43259  M,E    ****************************************

To CONTINUE, press Enter.
To PRINT this list of minidisks, press F4.
```

The minidisks command provides for the creation and destruction of VRM-maintained hard-disk partitions.

PHOTO 3: *Usability Services Menu Screen*

```
»UPDATE  »SWITCH  »ENVIRONMENT  »CREATE  »SORT  »PICK        »CLOSE
                          FILES
  Last UPDATE at 11:03.

  Current Directory is /usr/bin.

 »(root)  »usr  »bin

  Name           File Type    Changed    Size (bytes)

 »300            Run File     06/20/86     9764
 »300S           Run File     06/20/86     9840
 »300s           Run File     06/20/86     9840
 »4014           Run File     06/20/86    16840
 »450            Run File     06/20/86     9492
 »activate       Run File     06/18/86    49880
 »actmngr        Run File     06/18/86    51480
 »actwind        Run File     06/18/86   276492
 »archive        Shell Proc   06/18/86      548
 »at             Run File     06/20/86    37524
 »awk            Run File     06/20/86    75456
 »batch          Shell Proc   06/20/86       37
 »cancel         Run File     06/18/86    49880
 »cb             Run File     06/20/86    24604
```

The Usability Services user can open and view multiple command menus in switchable, full-screen environments.

dent AIX file systems can be grafted into the system's directory tree using the **mount** command in the same way that most UNIX systems accept the grafting of entire disk devices.

HIDDEN COMPLEXITY

Most UNIX environments split their user communities quickly into two groups: the high priests who choose to learn every detail of manipulating file systems, reconfiguring devices, and arranging intersystem communications, and all of the others, who do not. AIX developers took great pains to avoid baffling the latter group of users. This adaptation has all the special UNIX configuration files, but it hides most of the complexity of managing them from the user by providing friendly, knowledgeable facilities, such as **devices**.

Having installed the standard contents of the root and user file systems, the first-time user next installs AIX's "Additional Operating System Programs," including the **INed** text editor, Usability Services, the Asynchronous Terminal Emulator, Multi-User Services, and Extended Services. These additional standard programs, with other, optional licensed program products from IBM, are installed using the AIX **installp** and **updatep** utility programs.

Installp is capable of more than just moving files from a diskette (or tape) onto the hard disk. Providing higher-level facilities than the standard UNIX file-level tape archiver (**tar**), **installp** treats groups of related files as parts of a single product that must be installed together or not at all. **Installp** incorporates some fundamental requirements of good system management that are ignored by facilities available in most UNIX environments.

First, **installp** can preserve a copy of a superseded program version, along with any of its supporting files, in a *save* directory. Second, it automatically captures a note that an installation has been made in a chronological product *history* file. Third, **installp** allows software product suppliers to provide a product-specific installation procedure to be executed automatically, as part of the installation process. This procedure, in addition to calling on AIX or user-supplied programs, can invoke a set of internal **installp** commands that perform functions commonly required during software installations. The internal commands include **inusave** (archive file that will be replaced), **inurecv** (recover archived files), and **ckprereq** (determine whether the environment is compatible and current with the product being installed). When it has completed its product-specific installation work, the installation procedure returns a code to **installp** indicating the further actions required to make the newly installed product usable. With this code, the procedure can call for cancellation, no further action, or combinations of an AIX restart, an AIX kernel regeneration, and a VRM restart.

Updatep, **installp**'s companion program, allows system managers to apply updates to installed programs on an apply/commit/reject basis. A system manager can *apply* a revision, allow users to try it, and then later indicate that it is to be *committed* (kept) or *rejected* (automatically backed out). **Updatep** forestalls common system configuration management mistakes by preventing the immediate destruction of superseded program versions or the application of a new batch of product changes if older ones are still pending. Like **installp**, **updatep** also captures history information concerning updates, and allows product suppliers to provide a product-specific update procedure that is able to call upon general AIX commands or a set of special-purpose commands implemented in **updatep**.

These two programs hold obvious benefits. End users benefit from the ease with which software products can be installed. System managers are spared the critically important but tiresome work required to keep clear records, maintain fallback capabilities, and generally keep the system running smoothly. Software vendors who correctly compose installation and update procedures will avoid hours on telephone support hot lines puzzling out customers' questions.

In most other respects, operating and managing an AIX system holds few surprises for those familiar with other UNIX environments. A **users** command assists in the creation, removal, and adjustment of system users. AIX users carry all the familiar UNIX attributes; yet unlike some environments, users can belong to more than one group.

AIX observes the UNIX convention of checking its file systems at IPL (initial program load) using the **fsck** file system checker. When things go awry, the **fsdb** (file system debugger) can be used to traverse and examine an ailing file system in byte-level detail and to apply direct, low-level changes to the file system's structure and contents.

A standard complement of system accounting capabilities is provided for connect time, process, disk, and printer use. A **chargefee** command allows sys-

tem operators to levy one-time charges for special services and materials.

Backing up and restoring file system data incrementally or en masse is accomplished in traditional UNIX style using **backup** and **restore** commands or, alternatively, using the **dd** (device-to-device copy) command. All of these commands can be performed using either diskettes or streaming tape. AT coprocessor minidisks are not structured as AIX file systems; therefore they must be backed up and restored using **dd**. Unlike **backup** and **restore**, **dd** processes data at the disk image level instead of processing it file by file.

A stand-alone shell and **backup**, **restore**, **dd**, **fsck**, **fsdb**, and other selected AIX commands are available as part of a minimal AIX operating environment on the bootable "Installation and System Maintenance" diskette as well as in the full AIX environment. The quick-booting maintenance diskette can be used as a convenience to system operators or as a last line of defense when file system damage prevents bringing up the full AIX system from the hard disks. When necessary, system operators can effect repairs even when they are not able to run AIX normally.

Standard AIX provides two methods of conducting intersystem communications. UNIX's **uucp** and **uux** are available for intersystem file transfer and remote command execution. They are accompanied, in AIX's *Communications Guide* document, by an extremely clear explanation of their mysterious set-up and operating procedures.

Instead of the standard UNIX **cu** program for terminal emulation, AIX offers its asynchronous terminal emulator (**ate**) program. **Ate**'s interactive, menu-driven style is much friendlier than **cu**'s, and provides a much larger range of functions. **Ate** can emulate a VT-100 terminal, maintain a dialing directory and deliver dialing commands to a modem, and perform XMODEM or pacing-style file transfers.

DYNAMIC CONFIGURATION

With help from the underlying intelligence of the VRM environment, AIX allows dynamic configuration of its device drivers. At system boot time, the AIX kernel and its device drivers are loaded into system memory. Under the split-function AIX/VRM architecture, however, this accomplishes only part of the job of loading device support. Low-level, hardware-manipulating device intelligence actually lies in VRM's device drivers, which are not loaded automatically when AIX boots.

After the AIX kernel has initialized itself, the **/etc/rc** system initialization script invokes the **vrmconfig** program to load VRM's starting set of device drivers. **Vrmconfig**'s actions are controlled by the contents of two standard system configuration files: **/etc/system** and **/etc/master**. These two text files contain information, grouped into stanzas that indicate which drivers are to be loaded and how they are to be configured. **Vrmconfig** uses this information to issue Define Code VRM calls; with the assistance of "customize helper" programs it also issues Define Device calls and binds the VRM drivers to their AIX counterparts. When **vrmconfig**'s job is done, a fully operational set of device drivers is in place.

In typical AIX environments, device driver configuration is performed in a single burst of activity at boot time. AIX and VRM, however, are capable of loading or removing drivers later, during the course of normal system operation. Software vendors consequently have the option of providing VRM device drivers on a load-as-needed basis.

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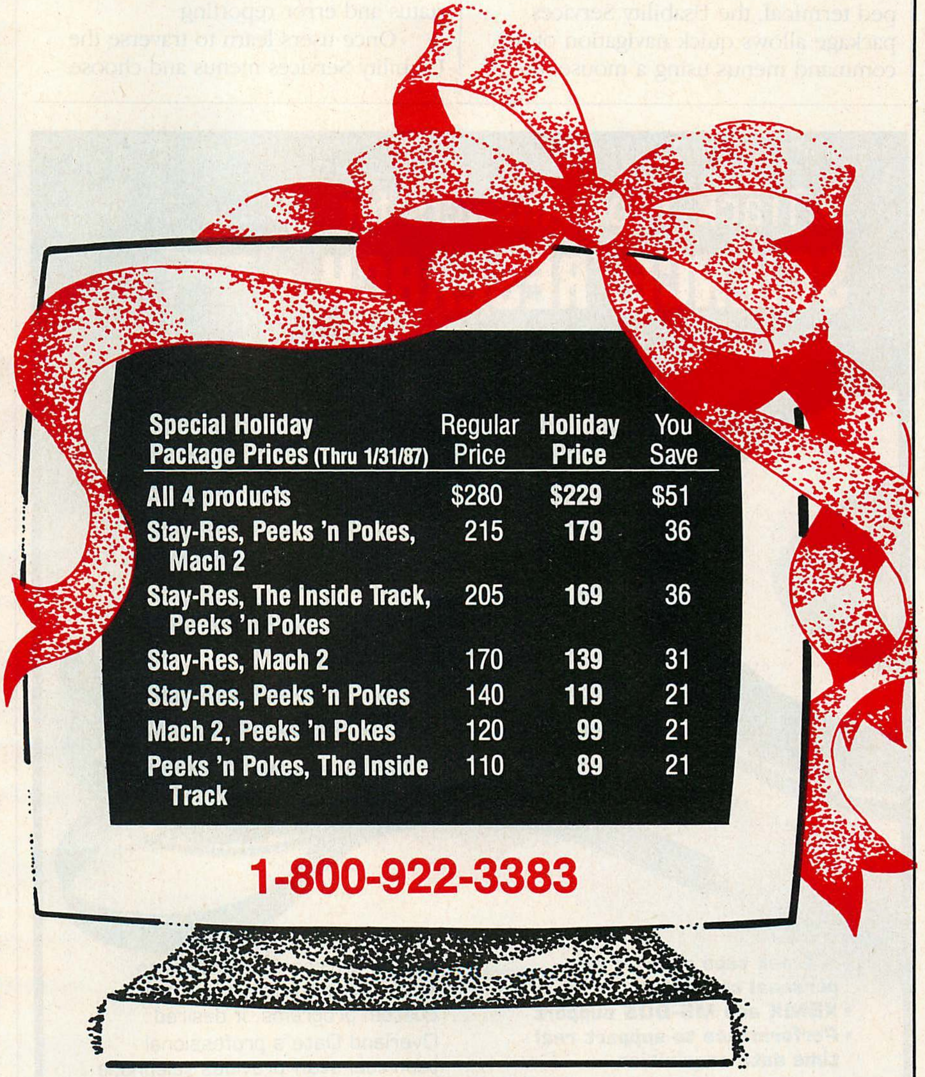

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AIX FOR BEGINNERS

IBM provides a set of programs and tutorials for first-time users in its Usability Services package, which allows users to interact with AIX in a menu-driven, pop-up window style. The services conceal UNIX's cryptic command names, for example, allowing users to **show** files instead of **catting** them, or to **find text** in files instead of **grepping** for it.

When used from a suitably equipped terminal, the Usability Services package allows quick navigation of its command menus using a mouse, the keyboard, or both. Just as shell-level users can create new instances of virtual terminals at will, Usability Services users can open and view multiple command menus in switchable, full-screen menus (see photo 3). From the services' top-level screens, users can open submenus for file management, DOS-style command processing, program development, communications, system configuration and customization, and status and error reporting.

Once users learn to traverse the Usability Services menus and choose operations, they can engage AIX in a much friendlier dialogue than the UNIX shells provide. However, like most menu-based systems, Usability Services slows down experienced users. UNIX novices who use the system often can wean themselves quickly away from the Usability Services environment.

DEVELOPMENT ENVIRONMENT

AIX *is* UNIX System V. Software developers familiar with standard UNIX will find an instantly familiar environment in the Bourne and C shells, the **vi** text editor and its variants, an optimizing C compiler, and the whole host of UNIX filters and utility programs.

The first AIX extension to the standard UNIX environment that users are likely to notice and exploit is its ability to create multiple virtual terminals on the RT's direct-connection, high-function terminal devices. By giving the **open** command, high-function terminal users can create and activate a new virtual terminal. **Open**, which takes the name of a command as an argument, creates a process to run the specified command and hooks its input and output streams to the newly visible terminal screen. For example, the command **open csh** clears the screen and shows the C-shell's prompt at the top. Users may work with this new shell and terminal until they terminate the shell by logging out, at which time the original screen (the one showing the **open** command) reappears.

If more than one virtual terminal is active (as many as 16 may be created at one time), AIX considers them to be members of a circular *terminal ring*. By using the Alt-Action key sequence, users can view the various virtual terminal screens. Terminating a virtual terminal's associated process causes the terminal to deactivate and drop out of the ring. If the RT's optional AT coprocessor is started, it creates its own virtual terminal as part of the ring and makes it the visible terminal.

Software developers can put virtual terminals to good use. By performing text editing on a different virtual terminal instead of in a process subordinate to the shell, developers can toggle from the editor back to the shell to browse files or run test or utility programs. Some processes that users normally would run in the background of a standard UNIX environment can be run under a shell on another virtual terminal, allowing users to continue their foreground activities while preserving the background's terminal output on its own, dedicated virtual terminal screen.

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In designing AIX's user interfaces, IBM's system developers paid special attention to experienced DOS users. By invoking the program **dos**, AIX users can place themselves in an uncannily DOS-like environment. Familiar command prompts appear, batch files work properly, DOS environment variables become defined, and device names such as A: and PRN: become usable. In fact, all of the standard DOS commands except BREAK, CTTY, EDLIN, EXE2BIN, GRAPHICS, and SYS are recognized and work as DOS users expect. It is disorienting, however, that the commands can be used in either AIX or DOS file systems. This illusion of a DOS system is created by a conspiracy of the **dos** program and a set of DOS work-alike programs residing in **/usr/dos/bin**; all make use of the DOS Services library (which also is available for linking with user-developed utilities, and is described later in this article).

Because fundamental differences exist between AIX and DOS file systems, **dos**'s DOS commands do impose a few ground rules. The **dos** program requires, for example, that file names within an AIX directory be limited to 14 characters; those in DOS file systems are limited to 12. Files in DOS directories must all have unique names; those in AIX directories are permitted to have duplicate names provided that they differ in letter case, upper- or lower-.

AIX's **dos** provides a few commands that are not available under DOS. A **filetype** command can be applied to a file and reports whether it is an ASCII or binary file in an AIX or DOS file system. A **convert** command translates text files between AIX and DOS formats. In situations where DOS simply does not provide the correct command vocabulary, direct AIX commands can be "escaped" into **dos** command lines by introducing them with an exclamation point.

Although **dos**'s imitation of the DOS environment has some omissions and a few subtle functional differences, it is surprisingly close to the real thing. Using **dos**, AIX users with no knowledge of UNIX can carry out a wide variety of system control and file maintenance chores such as formatting diskettes, locating and copying files, sorting and manipulating text, and performing file backups and restorations.

In addition to the **dos** command, a small family of AIX commands allows AIX users to work with DOS file systems without changing environments. **Dosdir**, **dosdel**, **dosread**, and **doswrite** query DOS file systems, delete files, and copy files between AIX and DOS file systems. **Dosread** and **doswrite** each are capable of optionally translating between AIX and DOS text file line and file termination conventions.

ARMADA OF EDITORS

UNIX is said to have more editors than most newspapers, and AIX does nothing to refute the observation. IBM has, in fact, added still another member to the UNIX armada of editors. In addition to the stream-oriented **awk** and **sed**, line-oriented **ed** and **edit**, and ubiquitous **vi** and **ex** programs, AIX offers Interactive Systems' **INed** editor.

INed is a visual, screen-oriented editor with capabilities that extend beyond the maintenance of ordinary text files. Invoked as **e**, **INed** allows users to work primarily in insert mode, invoking commands by escaping them with the Action (*execute*) key or by striking Alt- or Ctrl-shift key sequences. **INed**'s human-factors engineering is better than **vi**'s in that it does not treat ordinary (unshifted) keystrokes as commands. **Vi**'s packed set of unshifted command keys allows users who drop unwittingly from insert into command mode to wreak havoc on their text. **INed** also permits individual users to define *profiles*, sets of default parameter and option settings that automatically take effect whenever they invoke **INed**.

INed's extended capabilities are many. It allows the opening of multiple editing windows on one or more files, splitting the screen horizontally, vertically, or both. In addition to performing ordinary text editing, **INed** allows users to create structured files containing embedded, hierarchical format information. **INed** supports word-processor style automatic word-wrapping and is capable of maintaining comprehensive file history information, thus allowing the reconstruction of previous document versions even after many generations of revisions. A set of companion filter programs lets users perform such utility functions as extracting a plain text file from a structured **INed** file.

One long-standing strength of the UNIX environment is that, despite its laissez-faire style of support for individual software developers, it offers configuration management, or source code control (SCCS) facilities for use in version management and project coordination and control. AIX standard software includes the full set of SCCS supporting programs, including **admin**, **get**, **delta**, **prs**, and **sccsdiff**. UNIX's standard version- and dependency-minding **make** facility is also provided.

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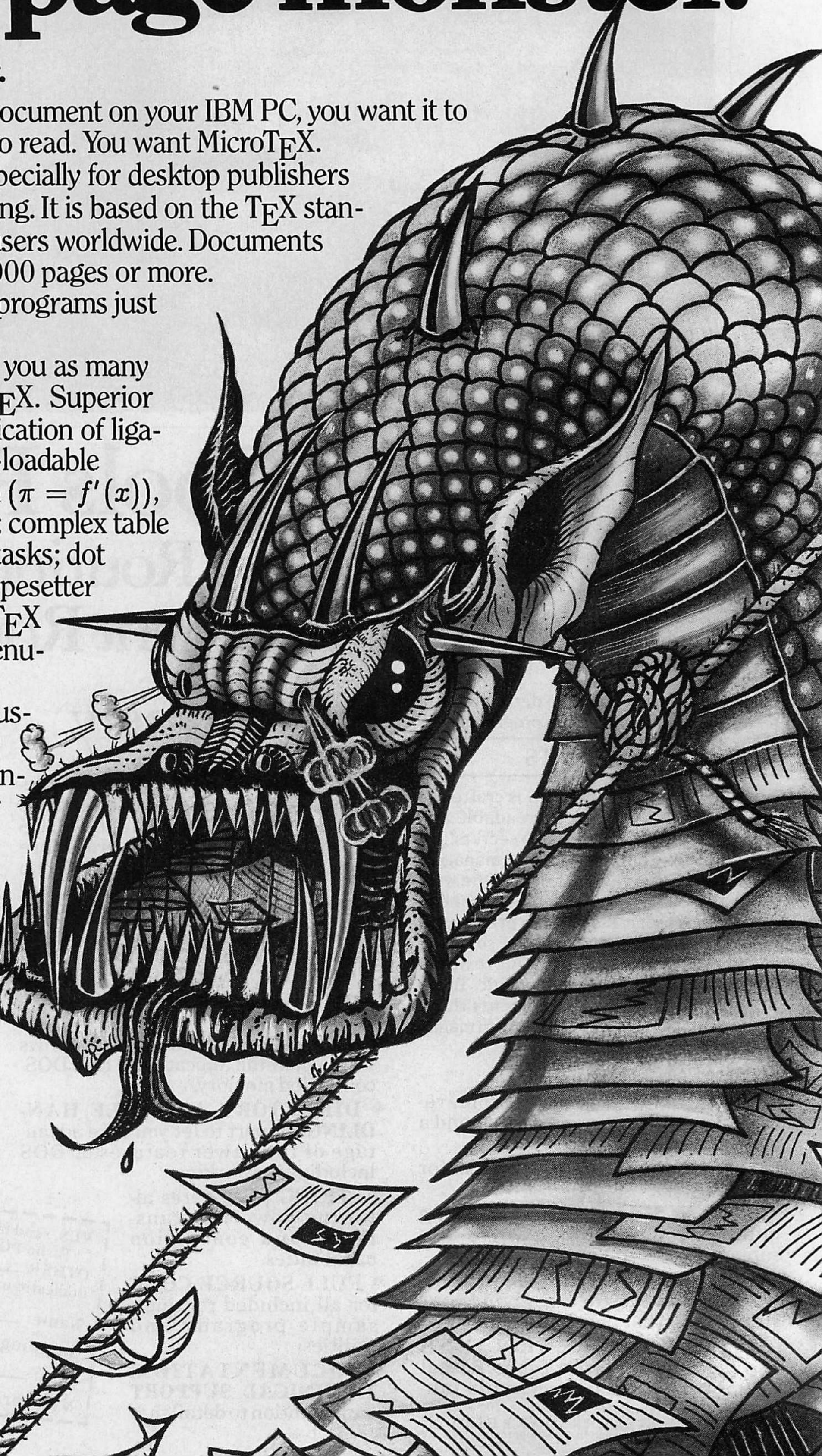

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TABLE 1: *AIX System Calls*

access	ftruncate	pause	sigpause
acct	getgroups	pipe	sigsetmask
alarm	getpid, getpgrp, getppid	plock	sigstack
brk, sbrk	getuid, geteuid	profil	sigvec
chdir	getgid, getegid	ptrace	stat, fstat
chmod	ioctl	read, readx	stime
chown	kill	reboot	sync
chroot	link	semctl	time
close	lockf	semget	times
creat	lseek	semop	ulimit
dup	mknod	setgroups	umask
exec:	mount	setpgrp	umount
execl, execv, execle,	msgctl	setuid	uname, unamex
execve, execlp, execvp	msgget	shmat	unlink
exit, _exit	msgrcv	shmctl	usrinfo
fclear	msgsnd	shmdt	ustat
fcntl	msgxrcv	shmget	utime
fork	nice	sigblock	wait
fsync	open	signal	write, writex

AIX is an accommodating environment. The list of AIX system calls, except for a few RT-specific extensions, should be familiar reading for experienced UNIX users.

AIX's C compiler and linker offer a standard set of invocation options. The compiler can be invoked in an optimizing mode, can produce symbolic information for the debugger, and can generate direct code for the RT's optional Floating Point Accelerator. Operating parameters can be tailored for different target environments by adding entries (stanzas) to the global C configuration file /etc/cc.cfg. Directives in **cc.cfg** control which programs are invoked as the various compiler and linker phases, which compiler and linker options are set by default, and which libraries are referenced automatically during linking. AIX's standard **cc.cfg** file contains stanzas for compiling for the normal AIX runtime environment (**cc**), compiling for the Floating Point Accelerator (**fcc**), and compiling modules for integration into VRM (**vcc**). The documentation also contains a promise (unmet in AIX's first release) of an **scc** variation for preparing programs to run stand-alone, without the services of the AIX kernel.

Programmers have the **sdb** debugger at their disposal. This full-function symbolic debugger allows a user to view and control a program's operation at the source code level, in addition to providing the standard set of machine-level analysis and debugging facilities.

APPLICATION PLATFORM

Developers porting software, especially C software, from other UNIX systems will find AIX accommodating. The list of AIX system calls (see table 1) and C-callable runtime routines, except for a few RT-specific extensions, is familiar reading. Traditional UNIX companions such as the **curses** device-independent screen management package are available. The C compiler is standard among larger-than-eight bit machines with respect to data representation: **ints** as well as **longs** and **floats** are four bytes long, **shorts** are two bytes, **doubles** are represented in eight bytes, and pointers of all types occupy four bytes.

Predictably, IBM has taken more pains than other UNIX vendors have to allow the rapid transportation of DOS applications to the RT. Programs written in IBM PC BASIC, Pascal, FORTRAN, and C find equivalent or near-equivalent syntax and semantics under IBM's AIX language processors.

In porting DOS programs that work with disk files, developers face a choice. They can transliterate DOS file management calls into their UNIX stream-based or direct I/O counterparts, or they can take a shortest-path conversion approach by recoding to use AIX's special DOS Services library. The library provides transparent access to files in both AIX and DOS file systems. It serves double duty in the AIX environment in that it can be used from DOS programs ported to AIX in minimum-effort style, *or* it can be viewed as a convenient tool for building utility programs that operate with equal ease in either AIX or DOS file systems.

Under DOS Services, a DOS-style disk drive specifier (A:, B:, etc.) can be

TABLE 2: *DOS Services Routines*

dosassign	dosexecve	dosopen	dosstat, dosfstat
doschdir	dosfirst, dosnext	dospwd	dostouch
doschmod	dosfsync	dosread	dosunlink
dosclose	dosinit	dosrename	dosunopen, dosreopen
doscreate	dosmkdir	dosrmdir	dosustat
dosdup	dosmktemp	dosseek	doswrite

The DOS Services library allows AIX programs to manipulate files in DOS file systems transparently, by masking fundamental differences between AIX and DOS.

bound to an AIX directory, file, or device formatted as an AIX or DOS file system. By using this capability, programs can conveniently manipulate DOS file systems on diskettes, the AT coprocessor's minidisk, or elsewhere. Standard DOS device names such as PRN: and COM1: can be bound to an AIX file, device, or program and used transparently (behind-the-scenes AIX pipes accomplish the binding).

To use the DOS Services subroutines (see table 2), a program must first call **dosinit** to initialize the quasi-DOS environment. Unless overridden, **dosinit** prepares the environment by establishing a default correspondence between standard DOS device names (COM1:, LPT1:, A:, etc.) and AIX devices (/dev/tty0, /dev/lp1, /dev/fd0). Although they do not provide an environment exactly like DOS, the DOS Services library masks many of the fundamental differences between AIX and DOS file management. Line termination in text files (DOS's carriage return/line feed versus AIX's newline) is handled transparently. The **dosfirst** and **dosnext** routines for matching file names accept a DOS-like file name matching template and operate in DOS or AIX directories.

DOS Services still has some rough edges; as a package, it is more translucent than transparent. Files are not closed automatically when a process terminates, for example, and differences exist in the management of DOS environment variables across **exec** family program invocation calls. Programs that rely heavily on DOS system calls may require extensive reworking. In an appendix to the *AIX Technical Reference*, IBM publishes a comprehensive table of DOS function calls and their equivalent (or similar) AIX system calls and environment subroutines for users making DOS-to-AIX ports.

Developers porting DOS applications can use AIX's command-level DOS compatibility support, as well as the subroutines in DOS Services. An AIX program can execute a DOS batch file by using **exec** on AIX's **dos** program with the appropriate parameters.

Even developers who are not regarding AIX as the target for minimum-effort ports of software from other UNIX or DOS home environments can still explore some of its other innovative capabilities and extensions.

The **curses** facility, providing terminal-independent screen management in most UNIX environments, exists in three forms under AIX: standard, compatible curses, a one-window accelerated subset of the standard package, and extended curses. In addition to the basic display control and windowing functions provided by standard curses, AIX's extended package allows access to a wide range of display attributes,

including color and font. It implements new pane, panel, and presentation space screen management abstractions, supports box drawing, and provides an elaborate set of functions for reading and checking keyboard input in a terminal-independent fashion.

AIX programs have at their disposal the high-function terminal (**hft**) driver, which can be used to operate the RT's various direct-connection display devices such as the Enhanced Graphics Adapter or Advanced Monochrome Display adapter. One of these devices, when grouped with the system keyboard and locator (mouse), constitutes a physical high-function terminal.

Much as DOS's ANSI terminal driver creates the illusion to DOS programs that they are conversing with a standard ANSI terminal device, AIX's **hft** driver creates the illusion that AIX programs are conversing with a very nimble, multicolor, multifont device. The analogy is limited, though; the AIX driver's ability to maintain many virtual terminals in association with a single physical terminal has no parallel under DOS. The **hft** driver inherits most of its function from VRM's underlying capabilities. VRM's Virtual Terminal Resource Manager does most of the work of managing virtual and physical terminals.

To the application program, the **hft** appears like any other UNIX device, accessed by the standard suite of device driver calls: **open**, **close**, **read**, **write**, and **ioctl**. For the **hft**, however, the calls have a vastly expanded set of capabilities. Each time the device, **/dev/hft**, is opened, the driver creates a new instance of a virtual terminal. The terminal user can switch around the virtual terminal ring in round-robin style by using the Alt-Action key sequence. The controlling program, also, can directly control which virtual terminal is made visible to the terminal user, or hide selected virtual terminals, causing them to drop out of the user-selectable rotation.

Using an expanded set of **ioctl** options, a program can query a virtual terminal's set of devices, reconfigure it, and selectively set **echo** and **break** attributes for each character. It also is able to load a keyboard map that determines the character code or escape sequence that will be delivered by each key on the physical keyboard.

The **write** system call can be used to deliver escape sequences that control the terminal's speaker, keyboard LEDs, and locator thresholds. **Write** sequences also control character set (character code-to-display-code mapping), color palette, and font. For the APA-8 Advanced Monochrome Display, fonts are selectable from a set of five IBM-supplied soft descriptions that are configured into VRM at AIX IPL time. Developers may configure and select other fonts of their own design using VRM's dynamic configuration capabilities.

All of these capabilities are accessible when the **hft** is operated in its default KSR (keyboard send and receive) mode. An additional MOM (monitored) mode exists that provides application programs with a short-circuit data path to and from the terminal. Under the faster MOM, terminal output can be performed directly to the display adapter via the system bus, and locator and keyboard input is taken from a ring buffer, bypassing the **read** system call entirely. From an application developer's viewpoint, the price of using the more efficient MOM is device dependence—programs using MOM must contain embedded knowledge of particular display adapters' interface characteristics.

AIX incorporates the System V Kernel Extension for interprocess signaling, coordination, and resource sharing, and, in fact, goes beyond the AT&T-specified extension in several respects. System V's standard **alarm**, **kill**, **pause**, and **signal** primitives are augmented by **sigblock**, **sigsetmask**, **sigpause**, **sigstack**,

and **sigvec**. By making use of the AIX extensions, processes can selectively block, ignore, or mask incoming signals, specify default actions to be taken by the system upon receipt of an incoming signal, or specify a special stack on which all signal processing is to occur. AIX's internal kernel-to-process signaling also has also been enhanced.

Communication of data and control information among AIX processes can be accomplished using families of extended AIX system calls for managing semaphores, message queues, and shared memory segments. Semaphores implement variants of the standard Dijkstra synchronizers that allow the passing of multiple resource units in a single operation. They are well integrated with the AIX environment; waiting processes still can catch signals, and a process's termination causes automatic cleaning up of semaphores with which the process was involved. A dying process that holds units of a semaphore's resource, for example, automatically frees them when it expires.

AIX provides a set of extended System V system calls for manipulating message queues that are shared among processes. Using the primitives **msgctl**, **msgget**, **msgrcv**, and **msgsnd**, asynchronous processes can engage in synchronized communication of multiple-type, variable-length messages.

AIX processes can communicate in a less structured way by allocating and arranging to share memory segments. The system calls **shmat** (shared memory attach), **shmctl** (control), **shmdt** (detach), and **shmget** (get or create) accomplish shared memory segment operations. The **shmat** call also can be used in one important variation. If it is passed an open file descriptor instead of System V's usual unique **key** identifying interprocess structures, it maps the descriptor's entire associated file into the calling process's address space. Files can be mapped in under read, read/write, or copy-on-write modes. In copy-on-write mode, changes to the file's image in memory are made only when (and if) the mapping process calls **fsynch**. In read/write mode, any modifications the mapping process makes to the file's image in memory are automatically reflected in its disk image.

In addition to providing program developers with the potential coding convenience of treating files as memory arrays, file mapping allows programs to cache the contents of frequently referenced files in memory without needing to expend any effort at the application design or coding levels.

A UNIX FOR EVERYONE

It is probably safe to say that more effort was expended on the development of AIX than on any other UNIX port to date. The effort has made AIX more attractive than most existing UNIX environments to prospective users, operators, and software providers. In AIX's high-function virtual terminals, its Usability Services, its complete set of System V utilities, and its ability to mimic the DOS user interface, end users will find significant advantages.

Those charged with operating AIX-based RT systems will also find that AIX distinguishes itself. By packaging into expert helper programs, such as **devices**, most of the knowledge required to perform routine operational chores such as adding and changing users, restructuring file systems, and modifying the system's device configuration, AIX has demystified the task of running a UNIX system. The **installp** and **updatep** software maintenance functions make many of the complex and often-ignored requirements of good system management easy to meet. AIX and VRM error logging make the identification and tracking of system and device errors easier to manage for operators and hardware service people.

Software providers who are contemplating the construction of new UNIX-based products or the transportation of existing UNIX or DOS products to the RT PC can expect a compatible, extended System V environment *and* numerous extensions that can be used to good advantage. AIX's program-controllable virtual terminals, file mapping, and optional data management facilities can be exploited to provide extensive function to end users without significantly increasing an application developer's effort. Vendors who re-host DOS products to the RT can find porting aids that are unmatched in other UNIX versions. Any vendor who must package custom device support with a product can benefit from the AIX open system support for addition and dynamic configuration of device drivers, and *all* vendors can gain by using AIX's well-conceived system management tools for licensed program products.

The RT PC running AIX must be judged an excellent UNIX engine. The arrival of AIX is a milestone in UNIX's coming of age as a commercial base for workstation computers.

Richard M. Foard, a consulting editor for PC Tech Journal, *is manager of product development at RoadNet Technologies, Inc., located in Baltimore, Maryland.*

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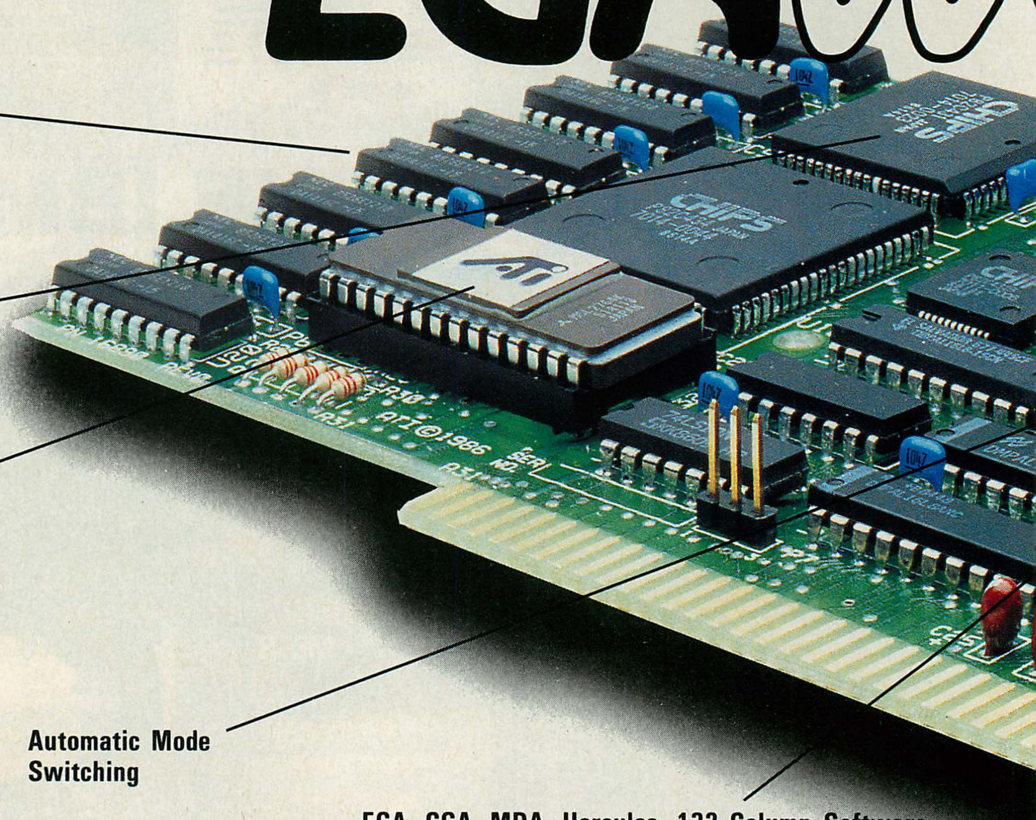

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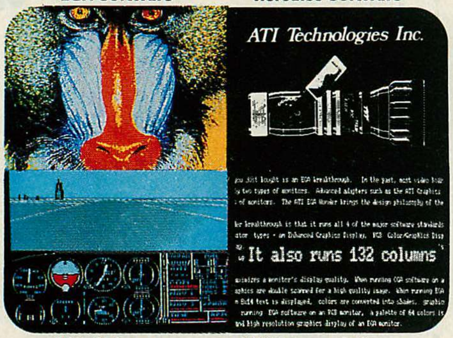
EGA Software | Hercules Software



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EGA Wonder runs EGA, CGA, MDA, Hercules and 132 Columns on an Enhanced Graphics Display. CGA text is improved to 8 ×14 and graphics are double scanned for a high quality display.

TTL Monochrome Monitor

EGA Software | Hercules Software

CGA Software | 132 Column Software

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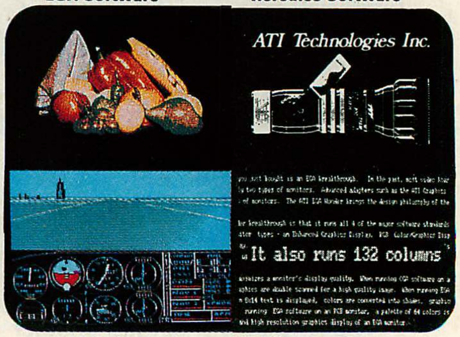
RGB, *Composite Monitors, and the IBM PC Portable

EGA Software | Hercules Software

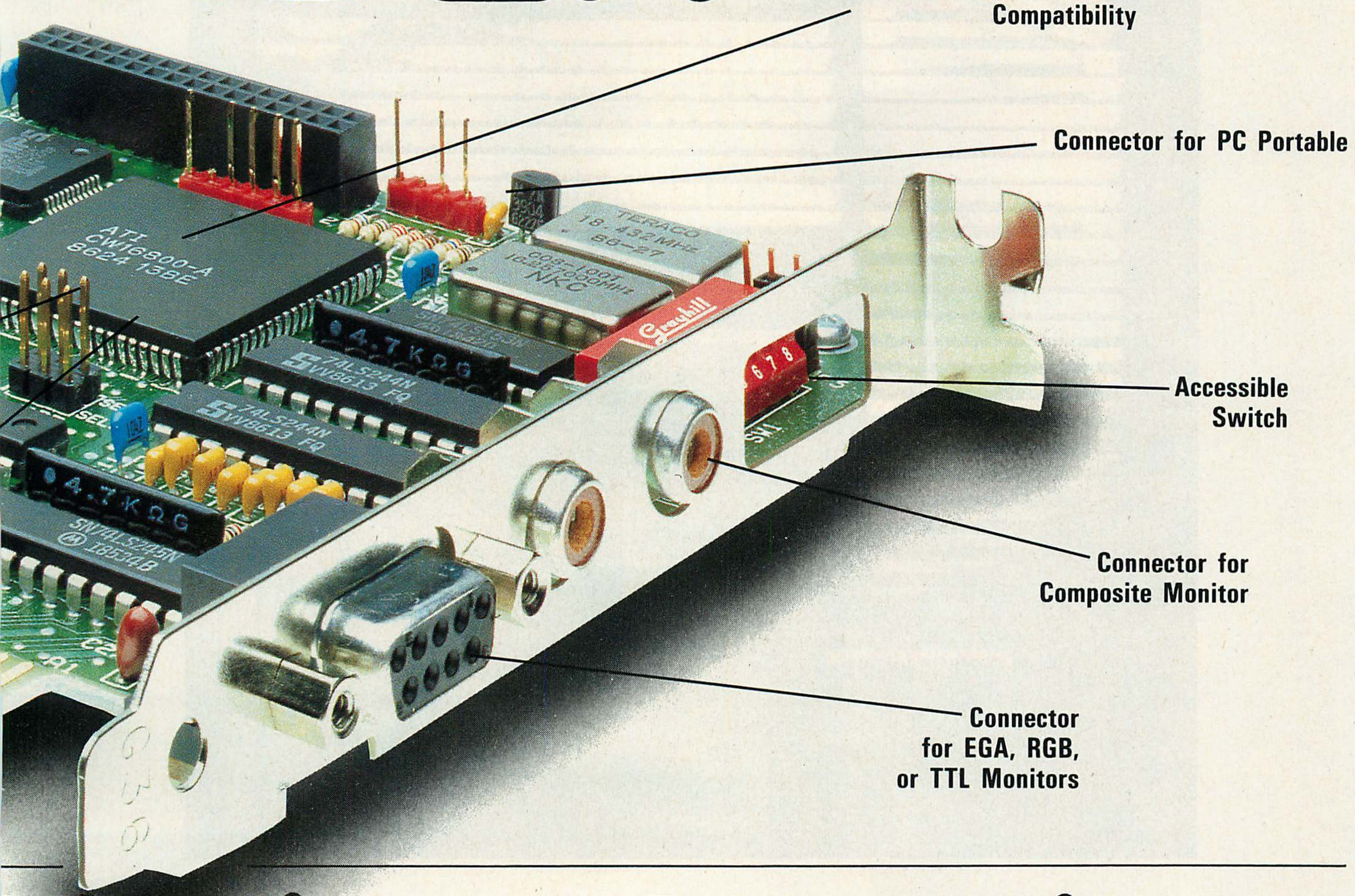


CGA Software | 132 Column Software

EGA Wonder also runs EGA, CGA, MDA, Hercules and 132 Columns on an RGB Monitor, *Composite Monitor, and the IBM PC Portable in 64 colors (shades). EGA and Hercules software are interlaced for high resolution text and graphics.

*Composite Monitor and PC Portable display not shown

ONDER



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Automatic Switching Between EGA and CGA Color Modes and Among EGA, MDA, and Hercules Modes	✓	✓	
Runs EGA, CGA, MDA, Hercules and 132 Columns on an EGA Monitor	✓		
Runs EGA, CGA, MDA, Hercules and 132 Columns on an RGB Color Monitor	✓		
Runs EGA, CGA, MDA, Hercules and 132 Columns on a TTL Monochrome Monitor	✓		
Runs EGA, CGA, MDA, Hercules and 132 Columns on a Composite Monitor	✓		
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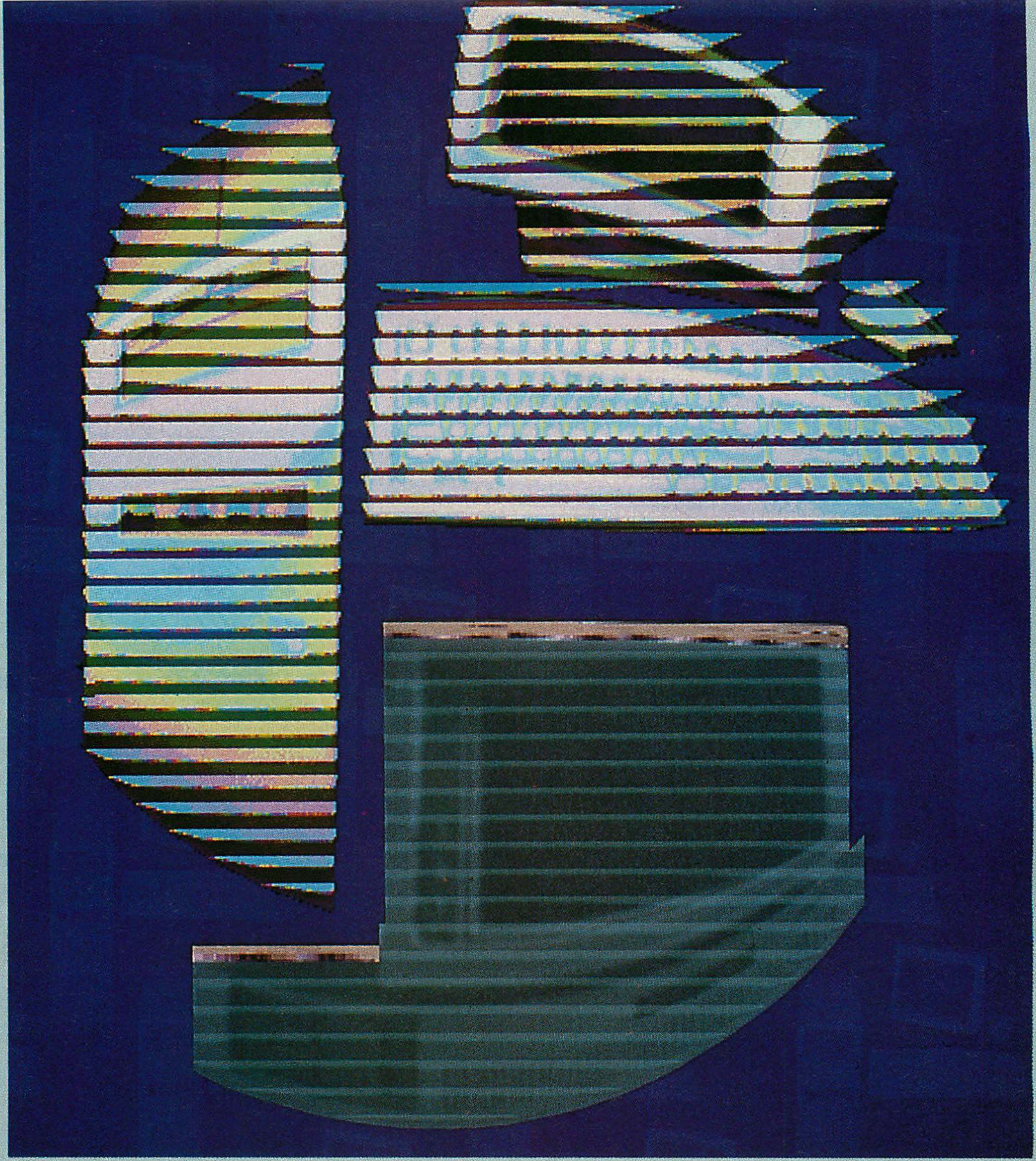

The Nearby AT

THOMAS V. HOFFMANN

IBM's AT Coprocessor Option puts an AT a keystroke away from the RT, providing a familiar environment for pre-RT software.

These days we expect any new box with PC in its name to be able to run all the PC spreadsheet, word processing, and flight simulator programs currently in favor. IBM's decision to use a completely new processor architecture in the RT PC means that it cannot run any of these programs on its primary processor, so how are our great expectations to be fulfilled?

IBM's solution is the AT Coprocessor Option, the essential ingredients of a PC/AT on a single adapter card, which costs approximately as much as an AT compatible ($995 for the coprocessor board plus $495 for the Coprocessor Services program). An RT outfitted with the AT coprocessor becomes two computers in one: a virtual memory RT and a standard AT. PC software is able to ex-

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ecute on the coprocessor concurrently with programs running in the RT processor, and both processors can share memory and peripherals.

The inclusion of an AT inside the RT is made possible by a combination of special hardware on the coprocessor board and software in the host processor that together emulate the functions of an AT. The resulting emulation is faithful, right down to soft rebooting with Ctrl-Alt-Del, which loads and executes whatever code is found on the diskette in drive A:. The coprocessor support software in the host processor uses the RT system's protection features to isolate other host programs from the effects of ill-behaved or not fully tested coprocessor programs.

USING THE COPROCESSOR

Before the coprocessor can play the part of an AT, a configuration must be established for the emulated AT system. The configuration includes the amount and type of memory and hard disk—in the form of VRM (Virtual Resource Manager) minidisks—to be allocated to the coprocessor, and the distribution of real and emulated devices, including at least one display. Devices can either be shared by both processors or dedicated to the AT coprocessor.

The AIX (Advanced Interactive Executive) command **pcstart** initiates coprocessor execution and sets the various configuration options, which can be saved in a customization profile and reused later. The user can allocate from 256KB to 640KB to the coprocessor in 32KB increments. Available memory in the I/O channel is used first. If more is required, it is allocated from host system memory and mapped into the coprocessor's memory map using the translation control mechanism on the RT system board. Directly accessed I/O channel memory provides the best coprocessor performance, but is more expensive than system memory and uses valuable slot space. The use of system memory degrades performance because the translation mechanism and the host memory management unit (MMU) are involved in every transfer.

Devices in the I/O channel may be assigned to the coprocessor only, the host processor only, or in some cases they may be shared. Devices dedicated to the coprocessor are handled solely by the coprocessor throughout the coprocessor session. Table 1 lists the ways in which supported devices may be used. In the case of displays, an additional *monitored* mode allows a display to participate in the VRM virtual terminal mechanism and be shared by the coprocessor and the host. Monitored mode also supports the emulation of the IBM Monochrome Display and Printer Adapter or Color Graphics Adapter using the new RT all-points-addressable (APA) displays.

The coprocessor's COM1 and COM2 devices can be disabled, assigned directly to serial adapters in the I/O channel, or redirected to one of two system board serial ports on the RT.

The diskette drives can be dedicated to the coprocessor, which directly accesses the diskette portion of the primary hard disk/diskette controller in the I/O channel. Other devices, such as network adapters, can be assigned to the coprocessor in a similar fashion.

All hard-disk I/O is handled by the host system. Up to two VRM minidisks (logical subdivisions of a physical hard disk) can be assigned to the coprocessor as drives C: and D: and can then be prepared and formatted using whatever AT operating system is desired. The DOS FDISK and FORMAT programs are used to prepare a DOS minidisk.

Once the coprocessor has been started, the RT keyboard and the designated primary display device become the coprocessor's keyboard and display. If the display is being shared, or if another display is assigned to the RT host, then the Alt-Action key combination can be used to switch to the next virtual terminal, moving from the RT to the coprocessor and back. The coprocessor session can be terminated by pressing Ctrl-Alt-Action or by entering the **pcend** command issued from the RT operating system AIX (if the active virtual terminal is an AIX console).

COPROCESSOR HARDWARE

The AT coprocessor card itself contains only some of the essential components of a real AT system board. The remaining elements are found on the RT system board or are emulated by host software. Special logic on the coprocessor card assists in emulating various functions and protecting the system from misbehaving coprocessor programs.

The coprocessor card includes a 6-MHz 80286 processor and associated crystal and timing logic; two 8259A interrupt controllers that provide 16 hardware interrupt levels; an 8254-2 timer/counter device; and the provision for an 80287 numeric coprocessor.

The DMA page registers, two DMA controllers, keyboard controller, and realtime clock/calendar resident on the RT system board are used indirectly by the coprocessor under the control and supervision of the RT's host processor.

Special interface and control logic on the AT board enable the host processor to perform these five functions:

- Trap I/O accesses by the coprocessor (in groups of eight using an 8K-by-1-bit RAM that is accessible by the host processor).
- Individually mask the I/O channel interrupts from the coprocessor and handle those interrupts directly.
- Simulate any of the available I/O channel interrupts by writing to a dedicated I/O address.
- Relocate the video buffer to system RAM and record in a queue the addresses in video RAM that have been written by the coprocessor.
- Stop and start the AT coprocessor and simulate a power-on reset.

These features are instrumental in supporting the emulation and control of various functions in a safe and relatively efficient way. Because the coprocessor shares the same I/O channel with devices that are assigned either to itself or the host processor, a mechanism is needed to control which processor sees which interrupts. The interrupt filtering logic can mask interrupts in the I/O channel from the coprocessor's view.

The I/O trap logic allows the host to set up the coprocessor to cause a host interrupt whenever it accesses certain I/O addresses. Then the coprocessor is stopped, and the host can read the data written for an I/O write operation or can supply the data to be read for an I/O read operation. Combined with the host's ability to force a coprocessor interrupt sequence, this procedure gives the host the ability to emulate any I/O device.

Emulation is required when the coprocessor attempts to access a device or function that is not present in the system, that is assigned to the host and is therefore unavailable to the coproces-

TABLE 1: *Device Support Modes*

DEVICE	ROMP	SHARED	DEDICATED	COPROCESSOR
MMU	●	○	○	○
IOCC	●	○	○	○
System mouse	●	○	○	○
DMA	○	●	○	○
Disk	○	●	○	○
Keyboard	○	●	○	○
Realtime clock	○	●	○	○
Configuration CMOS RAM	○	○	●	○
Display	○	●	●	○
Communications ports	○	○	●	○
Planar serial ports	○	○	●	○
Printer	○	○	●	○
Diskette	○	○	●	○
Speaker	○	○	●	○
New devices	○	○	●	○
System memory	○	○	●	○
I/O channel memory	○	○	●	○
80286's interrupt controllers	○	○	○	●
80287 math coprocessor	○	○	○	●
Interval timer	○	○	○	●
Light pen	○	○	○	●

● = *Yes*
○ = *No*

Devices in the I/O channel can be assigned to the host processor only, the AT coprocessor only, temporarily dedicated to the coprocessor, or shared.

"*Adapted from* IBM RT Personal Computer Technology.

sor, or that is present in a different form from the one expected by the coprocessor program.

The coprocessor card contains no memory—not even the ROM containing BIOS and BASIC. Instead, the BIOS and BASIC are loaded into memory (I/O channel memory if available), which is mapped into the proper place in the coprocessor's memory address space. The BIOS supplied with the Coprocessor Services program differs from the BIOS in an actual AT: the hard-disk functions have been replaced by a shared memory mailbox interface to the coprocessor device driver in the host, which emulates the hard disk using VRM minidisks; minor changes have been made to the video routines to improve performance when emulating standard PC displays on the new RT graphics displays. This "ROM-less" BIOS saves space on the coprocessor board and allows for future upgrades to be provided on diskette. This is important for issuing simultaneous changes to BIOS support for emulated devices and the host-resident emulation drivers.

DISPLAY SHARING

Dedicating a display adapter to either the host or the coprocessor is a straightforward matter. A display owned exclusively by the coprocessor is accessed directly through the I/O channel. The Coprocessor Services software must set the coprocessor I/O trap and interrupt filtering logic to permit direct access to the display I/O registers, and it must set the system address translation logic to permit access to the video refresh memory. Conversely, host-exclusive displays can be protected from access by the coprocessor.

A more difficult situation arises when a single display device must be shared by both processors, especially when both are executing concurrently. A further complication is the need to emulate standard PC displays on new hardware, for the benefit of old coprocessor-resident programs.

Display sharing is simple if alternating control between the host and coprocessor programs, with the invisible program dormant, is acceptable. The coprocessor can be stopped when it does not own the display, and the host tasks that need the display can be suspended while they wait for access.

A better solution would permit the concurrent execution of coprocessor programs even when the console is assigned to the host, with some way to save the display accesses in an invisible area until the device is assigned to the coprocessor. To bring about this solution both display buffer accesses and I/O accesses to the display hardware must be monitored.

Two features assist in implementing this solution. The video relocation facility allows coprocessor accesses to portions of the video refresh buffer of the coprocessor memory (addresses 0A0000H through 0BFFFFH) to be mapped into another area of system memory. When this feature is activated, the host can directly address the real display hardware, while the coprocessor addresses an independent buffer elsewhere in memory. The I/O trapping facility can be used to capture and record coprocessor changes to mode registers, cursor addressing, and other nonbuffer references. When the display is switched from one processor to the other, the buffers can be swapped and the display image restored.

The video redirection feature also allows for the hardware to store the address of each location written in the virtual display buffer in a separate area managed as a circular queue. This information can be used when restoring the display image from the virtual buffer in order to avoid processing the entire video buffer; only those locations that have been changed since the last update need to be processed.

The video address queue is especially helpful with an APA display, such as the RT Advanced Monochrome or Advanced Color display, which is emulating a character display such as the PC monochrome display. In such a case, the coprocessor writes only character codes and attribute bytes to the display buffer. If the emulation software had to reconstruct the entire display, pixel-by-pixel, from the character codes each time a key were typed, the performance would be totally unacceptable. By limiting the work done to what is necessary, the APA displays are acceptable substitutes for their predecessors.

80-PERCENT PERFORMANCE

IBM claims that the AT coprocessor will run about 80 percent as fast as the original 6-MHz AT when using I/O channel memory. Because both the 80286 processor and the memory are running at the same nominal speed as in a real AT, the degradation is probably caused by the overhead imposed by the address translation hardware that maps channel memory addresses into 32-bit system memory. Further performance degradation—to the point that performance is only slightly better than that of a PC/XT—results if the coprocessor is

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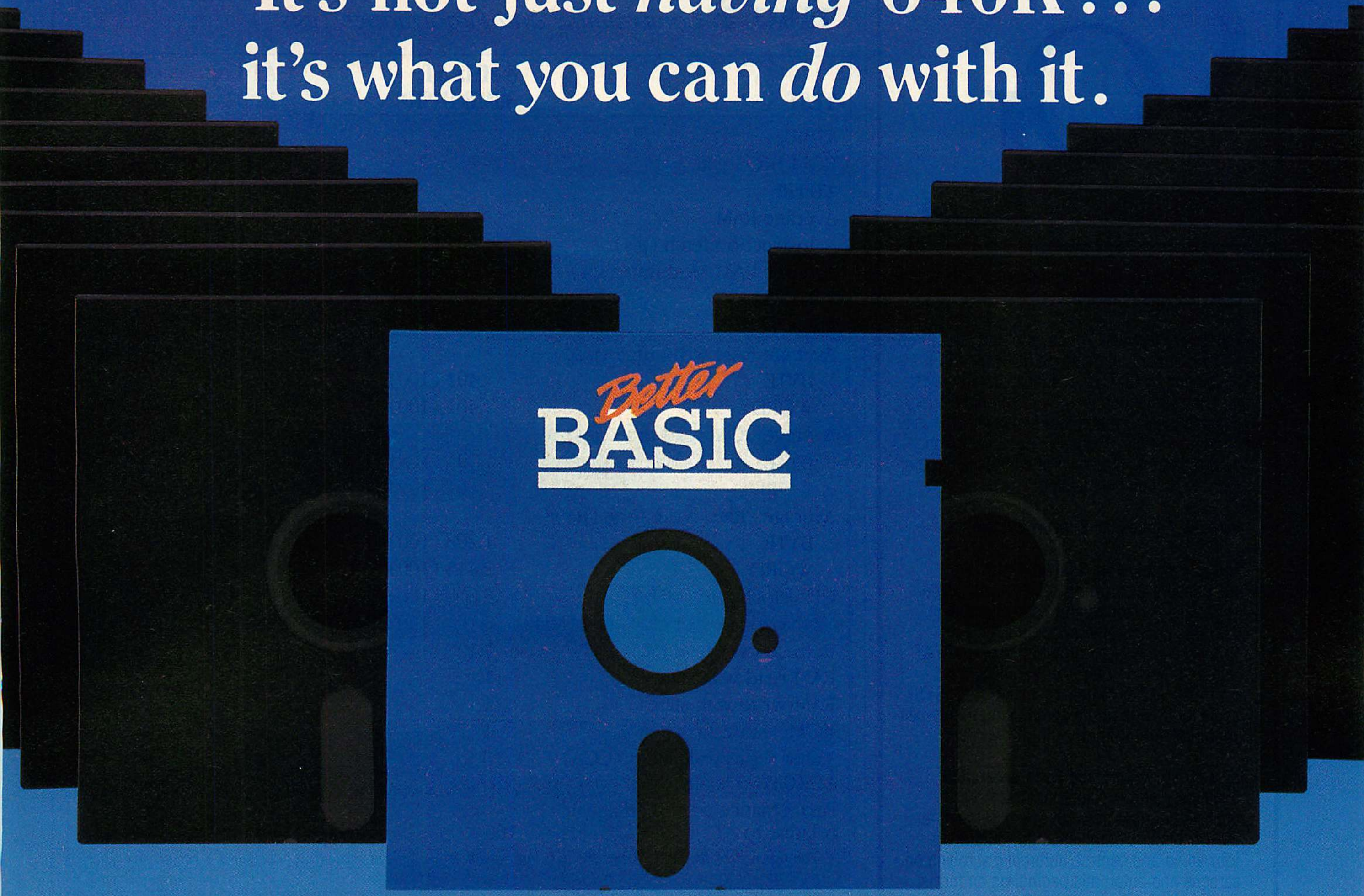

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TABLE 2: *Compatibility and Performance Tests*

TEST	8-MHz AT, 30MB DISK[a]	AT Coprocessor in RT
ATBIOS		
ROM BIOS date	11/15/85	10/15/85
ATPERF		
Average RAM instruction fetch (μs)	.403 (100)[b]	.718 (56)
Average RAM read time (μs)		
BYTE	.401 (100)	.708 (57)
WORD	.401 (100)	.707 (57)
Average RAM write time (μs)		
BYTE	.401 (100)	.710 (57)
WORD	.401 (100)	.708 (57)
Average ROM read time (μs)		
BYTE	.401 (100)	.708 (57)[c]
WORD	.401 (100)	.707 (57)
Average video write time (μs)[d]		
BYTE	1.208 (100)	.886 (272)
WORD	2.415 (100)	.887 (272)
CPU clock rate (MHz)	8.0 (100)	6.0 (75)
Math coprocessor clock rate (MHz)	5.3 (100)	4.0 (75)
Refresh overhead (%)	7.1	6.1
RAM read wait states	1	2
RAM write wait states	1	2
ROM read wait states	1	2
Video write wait states (CGA)	8	3
ATFLOAT		
Performance as percentage relative to AT	100	80

[a] *The figures for the IBM AT are the average results from several machines, whereas the results from the AT coprocessor are taken only from the review sample model.*
[b] *Figures shown in parentheses represent the relative performance expressed as a percentage compared to the* PC Tech Journal's *baseline machine, the 8-MHz, 30MB AT.*
[c] *Note that there is no ROM in the AT coprocessor; ROM reads are actually redirected to RAM.*
[d] *The IBM AT was tested with the CGA configuration. The RT AT was tested with Enhanced Monochrome Display with no CGA emulation.*

IBM's AT coprocessor option for the RT delivers approximately 60 percent of the performance of an actual 8-MHz AT (or 80 percent of a 6-MHz AT).

actually using system memory. This is due to the additional overhead of virtual address translation in the MMU and competition with the host processor for access to system memory.

Another negative performance factor is imposed when the coprocessor is using an APA display to emulate a PC character mode display, especially the PC Color Graphics Display. This emulation requires more time than the native displays and also steals most of the host processor resource.

Table 2 shows the results of the *PC Tech Journal* AT Evaluation Suite (these compatibility and performance tests were originally prepared for the *PC Tech Journal* series on AT compatibles; see "Out from the Shadow of IBM," Steven Armbrust, Ted Forgeron, and Paul Pierce, August 1986, p. 52). The tests were run on a Model 20 RT with 512KB I/O channel memory, using the RT Advanced Monochrome Display without color/graphics emulation. Note that the AT coprocessor environment has no ROM; ROM reads are redirected to RAM and take the same amount of time as RAM reads. Memory access times doubled when the tests were run with the I/O channel memory removed. The results are consistent with IBM's predictions, in that the coprocessor delivers 60 percent of the performance of an 8-MHz AT, which is 80 percent of the performance of a 6-MHz AT.

THE ADJUNCT AT

To provide a compatible AT environment in a host system architecture so radically different from a real AT is an ambitious undertaking. IBM has managed to produce a solution that is almost indistinguishable from a real AT for most applications. The only drawback is in the slower performance.

While few would consider an RT system with the AT coprocessor pri-

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marily as an AT replacement, it is very convenient to have an AT equivalent, complete with favorite and familiar software, only a keystroke away. This is especially true at this point because the availability of standard PC application software for the RT is limited. Even if that situation changes (and it is by no means certain that it will), the incremental cost of the coprocessor feature may be substantially less than the cost of replacing several applications.

The AT coprocessor is smaller and less expensive than a completely independent AT system, and the display and device emulation support provides flexibility that is not otherwise available. The concurrent execution of the coprocessor and host processor offer some intriguing possibilities, such as keeping a communications program running in the coprocessor, while performing workstation activities at the same time on the host processor.

Unfortunately, the AT coprocessor has some serious drawbacks. The best performance is obtained with dedicated memory in the I/O channel, and that is only about 60 percent of an 8-MHz AT. Using system memory only, performance is closer to that of an XT. Many applications require a dedicated display adapter for acceptable performance; the coprocessor and related adapters can occupy half of the available I/O channel slots. An RT is an expensive home for standard PC adapters supporting standard PC applications.

RT systems entirely dedicated to special applications such as CAD/CAM, publishing, data acquisition, or process control will not benefit from the coprocessor; neither will multiuser systems that support small departments or work groups using AIX for UNIX-based applications or development. In these systems the coprocessor is likely to be irrelevant or to produce too much of a drain on system resources.

RT systems used as *personal* workstations are another matter. Here the availability of familiar software tools can be a real productivity advantage. The AIX DOS Services software provides convenient, direct access to DOS format files on diskettes or minidisks for sharing data between AIX and coprocessor applications. The AT coprocessor may not be *better* than the real thing, but in some cases it can be a useful adjunct to the RT workstation.

Thomas V. Hoffmann, a consulting editor for PC Tech Journal, *is manager of systems development at RoadNet Technologies, Inc., located in Baltimore, Maryland.*

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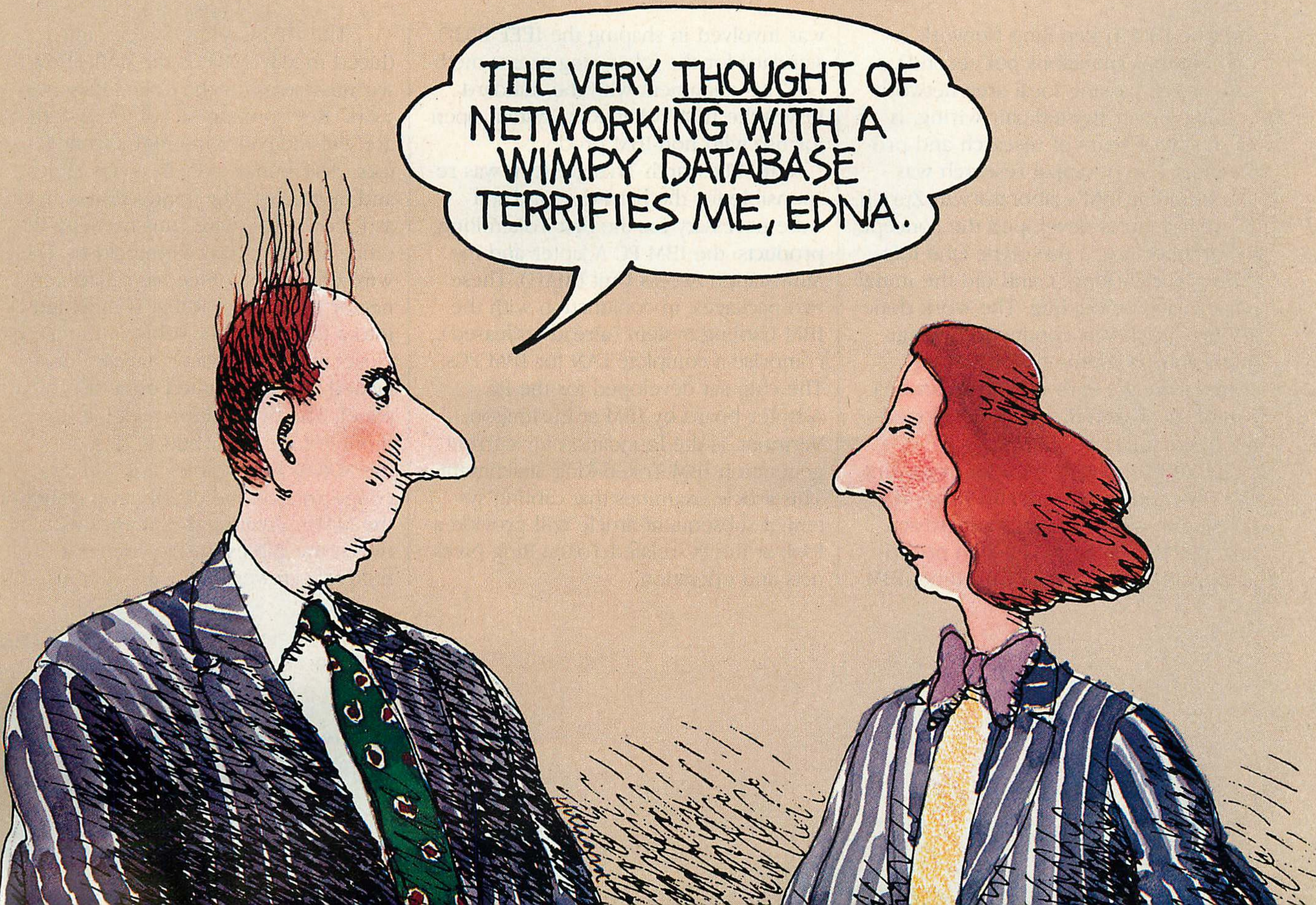
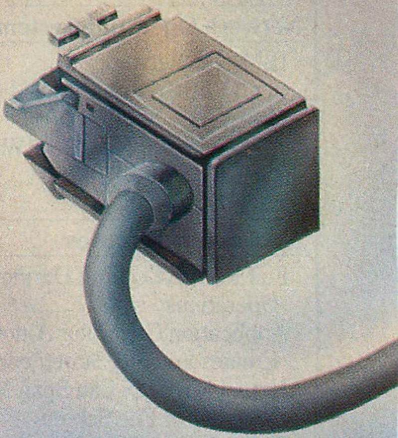


The key components of the IBM Cabling System are ready and awaiting the delivery of IBM's Token-Ring Network. Users can begin to install cabling according to individual communications needs.

Underlying Connections



J. SCOTT HAUGDAHL

The IBM Token-Ring Network, a 4-Mbps (megabits per second), token-passing local area network operating over twisted-pair wiring, is the result of years of research and prototyping. The principal research was conducted at IBM's laboratory in Zurich. There, scientists developed the concept, the architecture, a prototype (the infamous "Zurich Ring"), and did the initial performance modeling. The work done at IBM/Zurich was continued by engineers and programmers at IBM/Research Triangle Park in North Carolina where the Token-Ring was developed into a commercial offering.

IBM broke with tradition regarding the Token-Ring. Historically, it has remained aloof from IEEE standard-setting, electing to create its own proprietary product standards. This time, IBM was involved in shaping the IEEE 802.5 standard for the token-ring access method. This alignment with the standard leaves the IBM Token-Ring system open for use with non-IBM products.

IBM/Research Triangle Park was responsible for the hardware and software necessary for the first Token-Ring products: the IBM PC Adapter and the Multistation Access Unit (MAU). These two packages, in conjunction with the IBM Cabling System (already released), comprise a complete LAN for IBM PCs. The chip set developed for the PC Adapter board by IBM at Burlington, Vermont, is the foundation for current generation IBM Token-Ring attachments. This article examines that cabling system; a subsequent article will provide a look at the PC-related Token-Ring products and operation.

The IBM Cabling System, introduced in May 1984, is the underlying wiring system for the Token-Ring Network. Key components of the system are: twisted-pair wire, MAUs, connectors, distribution panels, patch cables, and faceplates. The connection is made as follows: The wire runs between the office and a central wiring closet. The wire end in the office has a data connector attached to it that is mounted into a faceplate. The cable in the wiring closet also has a data connector attached and is mounted on a distribution panel. The distribution panel, in turn, is mounted in a distribution rack above the MAUs. Patch cables link the data connectors on the distribution panel to the MAUs, creating the physical link between the cables. In the case of a small network—fewer than eight stations—the

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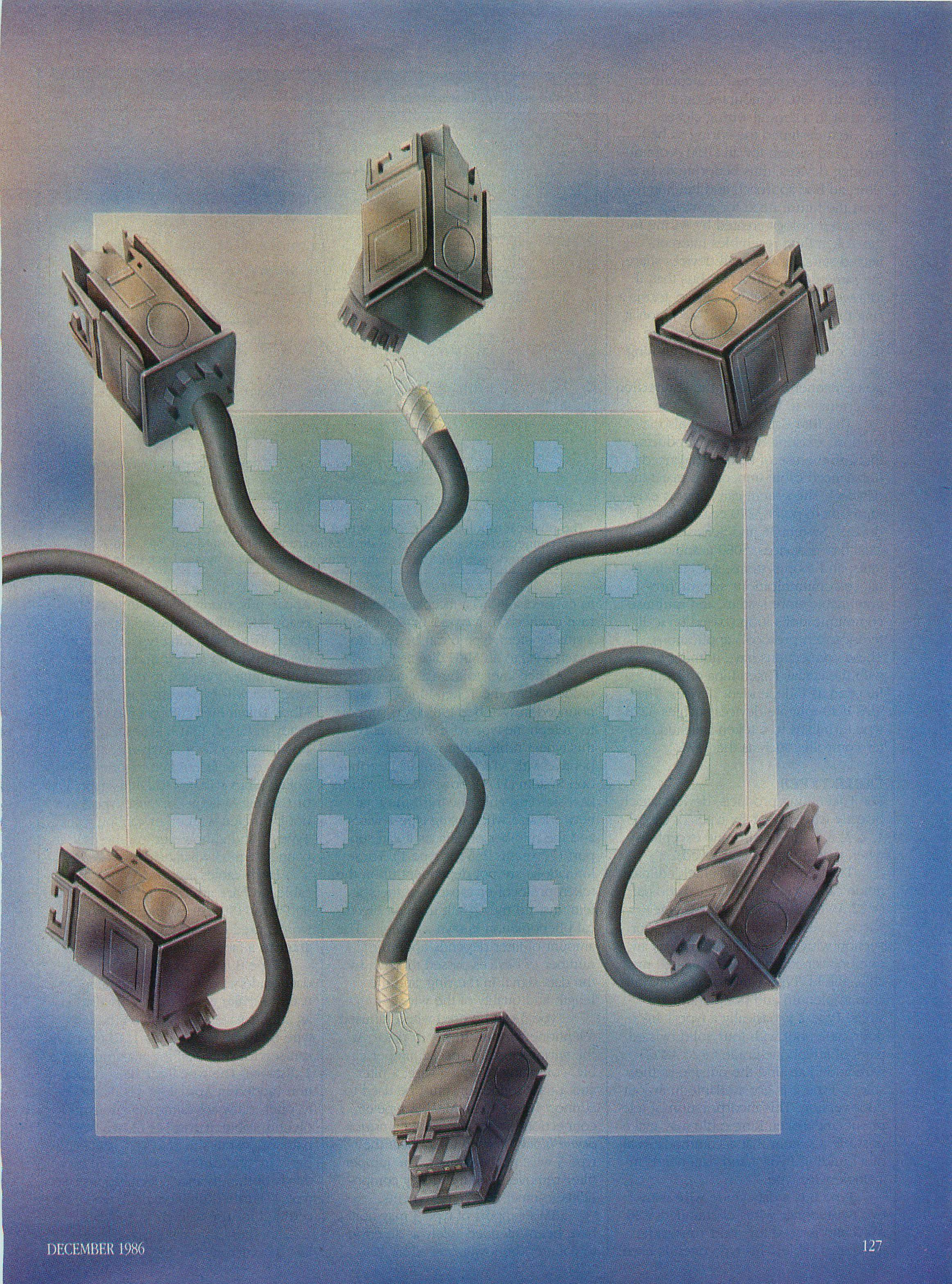
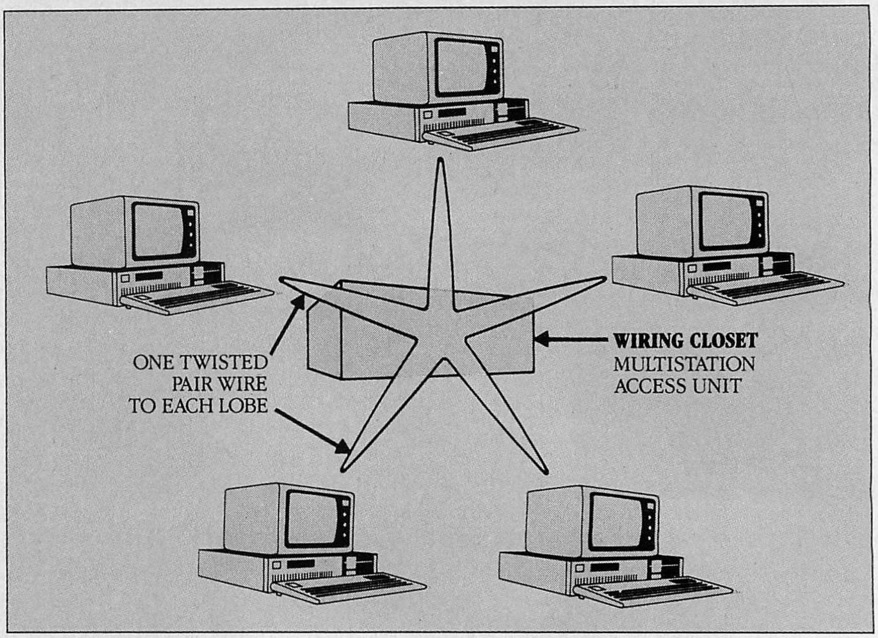


wires can be connected to a common point; the MAU is mounted on a wall instead of in a central wiring closet.

IBM designed the wiring to be a structured system for all (IBM) communicating devices, thus bettering its previous ad hoc approach and helping to avert the future need for rewiring. The physical topology created by wiring for the Token-Ring resembles interconnected stars, in which all devices share the same dual twisted-pair bus that, if followed from device to device, forms a ring that eventually wraps back upon itself (see figure 1). The cable can be used for more than simply Token-Ring devices; it can function in a point-to-point manner to support the connection of terminals to hosts.

The IBM Cabling System also supports existing nontoken products through the use of baluns (balanced-unbalanced cable impedance matching devices). The system can support existing point-to-point 3270 coaxial-based devices, System/36 and Series/1 twinaxial-based devices, 5080 graphics systems, and loop systems, such as the finance communications system, programmable store system, and multiuse communications loop (based on a different token protocol) applications. These connections have nothing to do with the actual Token-Ring and still function as independent devices. The idea is to migrate devices such as 3278-type terminals to a token-attached cluster controller such as the 3174.

FIGURE 1: *Token-Ring Topology*



The physical topology created by wiring for the Token-Ring Network resembles interconnected stars in which all devices share a dual twisted-pair bus, that if followed from device to device, forms a ring that eventually wraps back upon itself.

CABLE TYPES

For Token-Ring products, devices attach directly with one of six types of cable: 1, 2, 3, 6, 8, or 9 (with one exception when type 3 wire is employed).

Type 1 is an overall, shielded, data-grade cable with two solid twisted-pair (#22 AWG—American Wire Gauge) wires. Type 1 is available as an indoor version with a braided shield or as an outdoor version with a corrugated metallic shield. Type-1 indoor is also available in plenum and nonplenum versions. Type 2 is basically a type-1 indoor cable, but with four solid twisted pairs of telephone-grade (#26 AWG) wire added around the outside of the shield. Type 2 is not available in an outdoor version. This incorporation of telephone and Token-Ring cable may make possible a system that accommodates all of a building's voice and data needs in a single wire type.

Type 6 is a data-grade wire with two twisted-pair wires of stranded #26 AWG and is used for short runs as flexible patch cable. This type often is used to connect a PC to a faceplate that in turn connects to a type-1 or -2 cable. In a small system, type 6 can be used to attach a PC to an MAU directly.

A latecomer to the Cabling System (added when the Token-Ring was announced in October 1985) was support for telephone-type wire. Presumably, this type-3 cable addition is cost-competitive with AT&T's Premises Distribution System (PDS); however, it sacrifices LAN size (roughly one-third the total network size when using type-1 wire) and the number of devices it can support (72 versus 255 for type 1). These limitations are not dependent upon the token protocol or capacity of the system; instead they result from an electrical phenomenon known as "jitter." The amount of jitter depends upon the number of devices passed through by the data signal in the ring, and the length and quality of the wire.

Type 3 can be used where unused telephone wire is already in place. At the wiring closet, a special jumper cable, consisting of type-6 wire, a filter, and a data connector, must be used to connect type 3 to an MAU. A type-66 connection block (also called a *punch-down block*) is used to connect the type-3 wire to the jumper. The jumper filter removes high-frequency components to meet FCC requirements.

IBM's support of type 3 may not have been intended solely as an effort to counter the lower-cost AT&T PDS. Apparently, many IBM customers already had miles of unused type 3 in place. The Token-Ring type-3 support is designed to be ad hoc and temporary, with a migration path to the data-grade wire that will be required by future 16-Mbps Token-Rings. If type 3 is not already installed, IBM is discouraging its installation in favor of types 1, 2, 5, 9, and so on. In fact, two categories of Token-Rings will be available—type 3 or Cabling System—because type 3 cannot be mixed with other cabling types. Types 1 and 2, however, can be used to connect type-3 wiring closets together.

Patch cables are made with type 6 cable, and are available in lengths of 8, 30, 75, or 150 feet. A special 8-foot version is used to connect the IBM PC Adapter to a faceplate.

Type 8 is a #26 AWG twisted-pair data-grade wire with a plastic ramp used to make under-carpet installation as unobtrusive as possible. Although type 8 can be used similarly to type 1, it can service only half the maximum type 1 distance. The type-9 media specification (added in April 1986) is designed to offer a low-cost alternative to type 1 plenum cable. It consists of two twisted pairs of overall shielded #26 AWG copper wire and can operate at up to two-thirds of the distance specifications of type 1. Further, unlike type 3, type 9 is certified for use as high as 16 Mbps.

Another cable type, type 5, is a 140/100 micron-fiber cable designed to

interconnect wiring closets via repeaters. IBM has not yet announced support of fiber at the PC-interface level.

Table 1 summarizes the capability variations among the data-grade types 1 and 2 and the voice-grade type-3 wire. The drive distances are relative to type 1. The maximum drive distance (recommended by IBM) for type 1 is 300 meters from a wiring closet to a work area and 200 meters between wiring closets. These are absolute maximum distances that become shorter as the physical ring wiring becomes larger (as more and more wiring closets, MAUs, lobe wiring, and devices are added). The *IBM Token-Ring Network Introduction and Planning Guide* provides tables and formulas that can be used to calculate the maximum distances.

Designed specially for the Cabling System, the data connector is the plug that terminates all twisted-pair wire. Two data connectors can join together by a 180-degree rotation of one connector. Thus, only one type of data connector is necessary to make the connections. When two connectors are used, one of the connections is contained in a faceplate. Faceplates that contain RJ-11 jacks, necessary for connection of a telephone to the additional telephone wire contained in type-2 cable, are available.

TABLE 1: *Performance Capabilities of Cable Types*

	1	2	3	5	6	8	9
Drive distance[a]	1.0	1.0	0.45	3.0	0.75	0.5	0.66
Data rate (Mbps)	16	16	4	250	16	16	16
Devices per ring	260	260	72	260	260	260	260
Closets per ring	12	12	2	12	12	12	12
Voice support	No	Yes	Yes	N/A	N/A	N/A	No

[a]*These numbers represent the relative length of cable used for each cable type for any given hardware.*

Although the Token-Ring will permit existing telephone wire (type 3 above) to be used for the cabling system, the performance and size of the network is limited.

MULTISTATION ACCESS UNITS

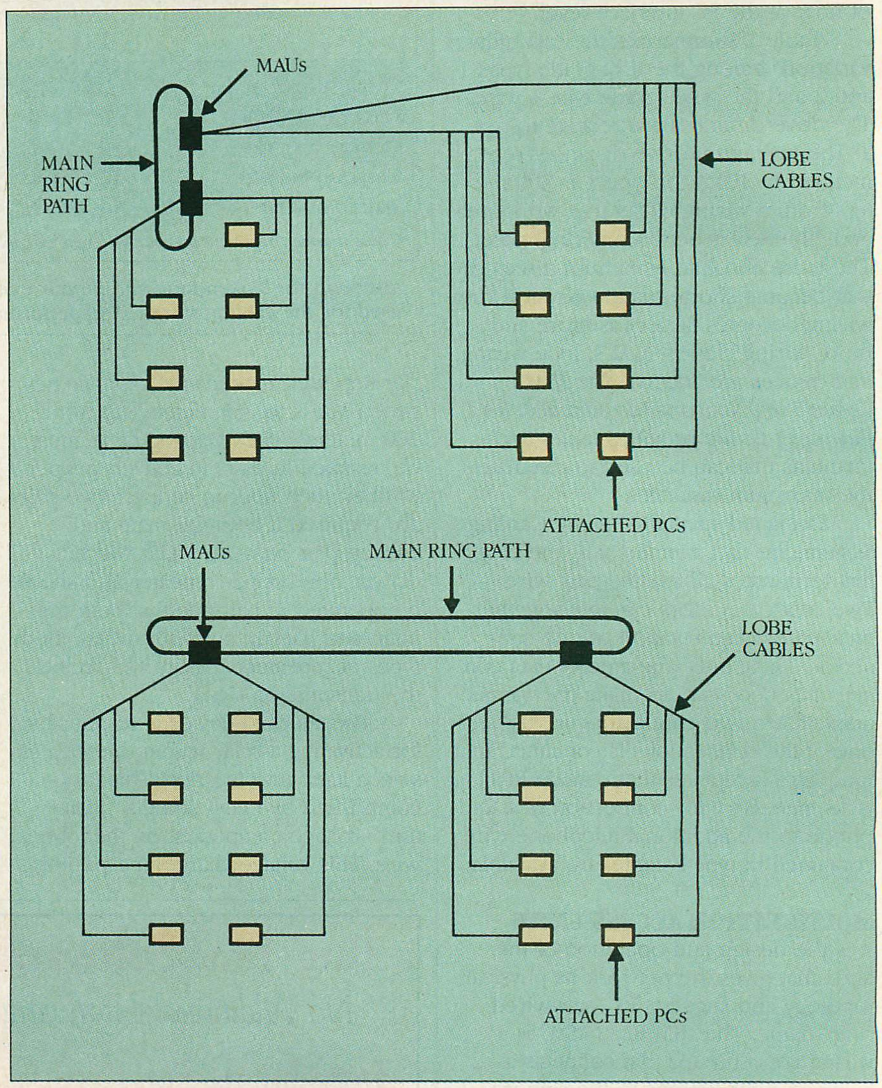
It is the design and operation of the MAU that gives the network its physical topology and suggests its "star-wired ring" name. The IBM 8228 MAU is a wiring concentrator that connects as many as eight stations to the ring via drop cables called *lobes*. A ring-in jack on one side of the MAU and a ring-out jack on the other side provide for a daisy-chained connection to other MAUs. The MAU provides for insertion/bypass of lobe segments and associated attaching devices. It can accomplish write/fault detection through the use of an attached device, such as the IBM PC Token-Ring Adapter. By configuring a ring that connects the last MAU to the first, a repetitive path is formed, because none of the MAUs is wrapping within the box. Under this configuration, any one cable between a pair of MAUs can be removed, and the ring will remain fully operational.

In order to increase the distances of the basic cabling system, IBM supports type-5 fiber media with the IBM 8219 Token-Ring Network Optical Fiber Repeater. This unit attaches to an MAU to extend the distance between MAUs to 2 kilometers. A repeater or copper-type media, the IBM 8218 Token-Ring Copper Repeater, extends the distance between MAUs to 750 meters (up from 200 meters). The fiber repeaters must be installed in pairs to convert copper to fiber, then fiber to copper. Two pairs are required if both the main and backup pair between MAUs will be driven. The copper repeater also should be operated in pairs, so that both the main and backup pairs are driven. Both types of repeaters amplify and reclock the transmission signal.

The attached device is responsible for activating a relay within the MAU to switch itself into the ring. This is accomplished by maintaining a "phantom" voltage component on the lobe wire. This voltage charges a capacitor on the relay, which then inserts the lobe into the network. When the device either fails or is turned off, the relay will deenergize and disconnect the device from the ring.

Although the relays automatically latch when devices are inserted or removed, a sudden jarring movement during the shipping of the MAU could cause a relay to be latched in the wrong state. IBM therefore includes a testing tool with the MAU. Insertion of the tool into the connected ring tests whether all relays contained are wrapping. If an anomaly is detected, the tool can be inserted into each lobe connection to test the associated relay's status and correct it if necessary.

FIGURE 2: *Multistation Access Units*



Adapted from IBM Token-Ring Network Introduction and Planning Guide

These two examples show how the MAU can be used to set up different physical configurations with the ring. In the first case (top), the MAUs are contained within a single room; in the second example, the MAUs are more widely distributed.

The MAU can be rack- or wall-mounted. The wall-mount feature requires an optional wall-mount housing, also available from IBM. Networks with eight or fewer nodes can use a single wall-mounted MAU with a maximum 150 meters of type-6 cable connected directly to the device or wall plate.

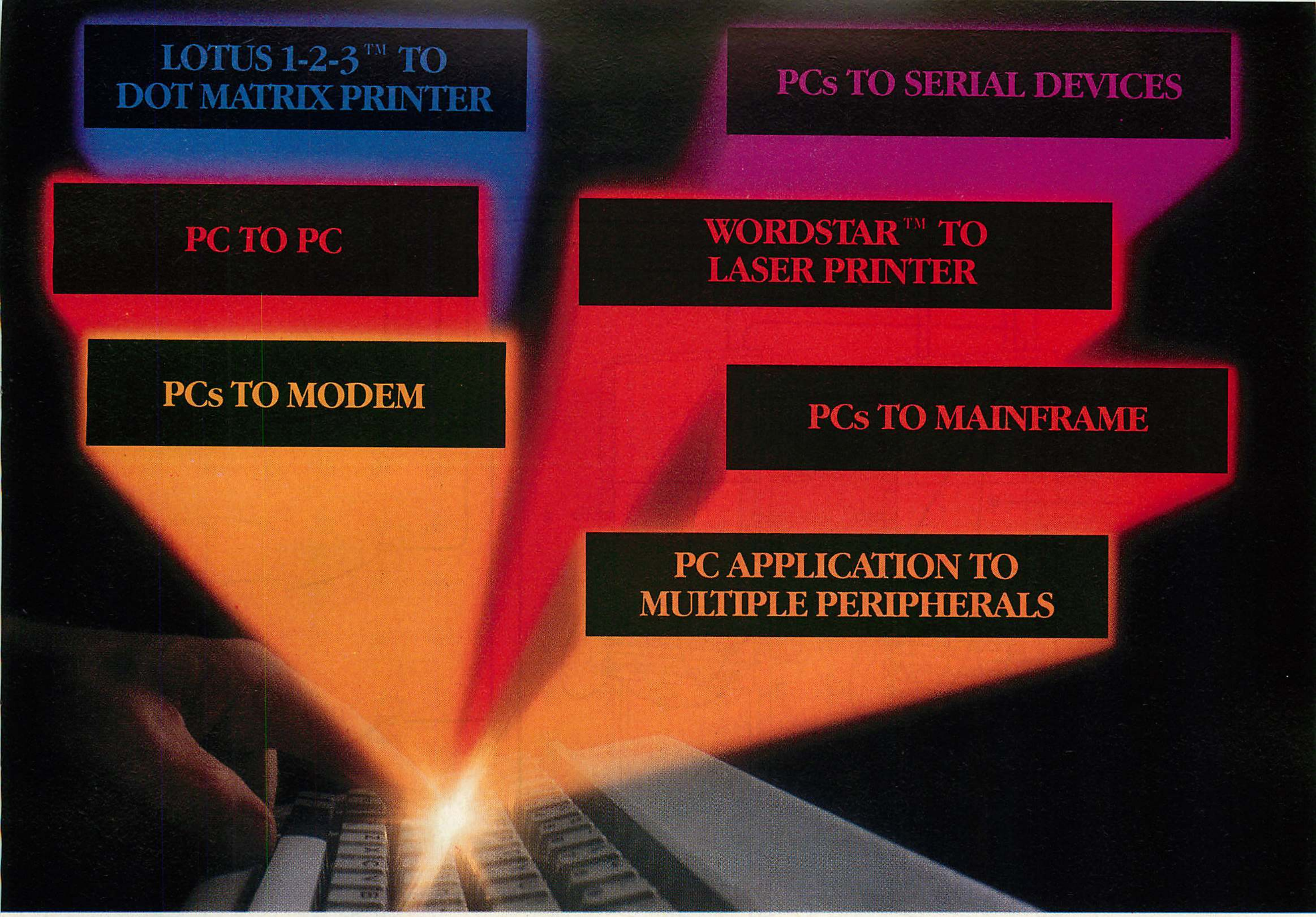
An interesting variation of the MAU is the 3Com RingTap, which is, essentially, a single-port MAU—that is, the physical topology could be configured as simply a ring, rather than a star-shaped ring. Although the wiring is simplified in the ring arrangement, it becomes difficult to manage (because it has no centralized isolation points) and adding new taps can prove disruptive.

At the other extreme, Ungermann-Bass offers an intelligent MAU called the Distributed Wiring Concentrator (DWC). The DWC offers 10 ports (excluding ring-in and ring-out) and can operate in active or passive (IBM MAU-compatible) mode. In its active state (power applied), the DWC allows the Ungermann-Bass Network Management Console (NMC) to perform problem determination, fault isolation, and, when appropriate, station removal from the ring.

WIRING CLOSETS

The MAU can be used to set up many different configurations of the ring. Figure 2 shows two examples of offices with PCs connected to two MAUs. In the first, the MAUs are located within one room (or wiring closet), forming a star-wired ring. In the second, the MAUs are more widely distributed.

A PC can be attached to an MAU using a type-6 patch cable and PC adapt-



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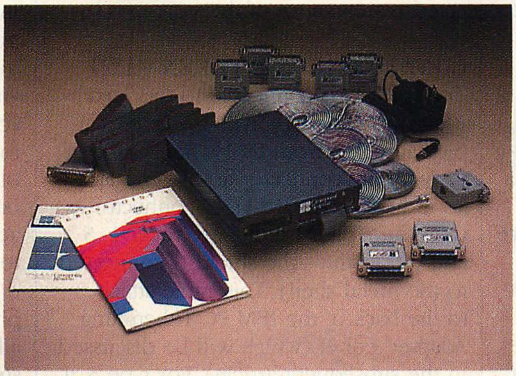

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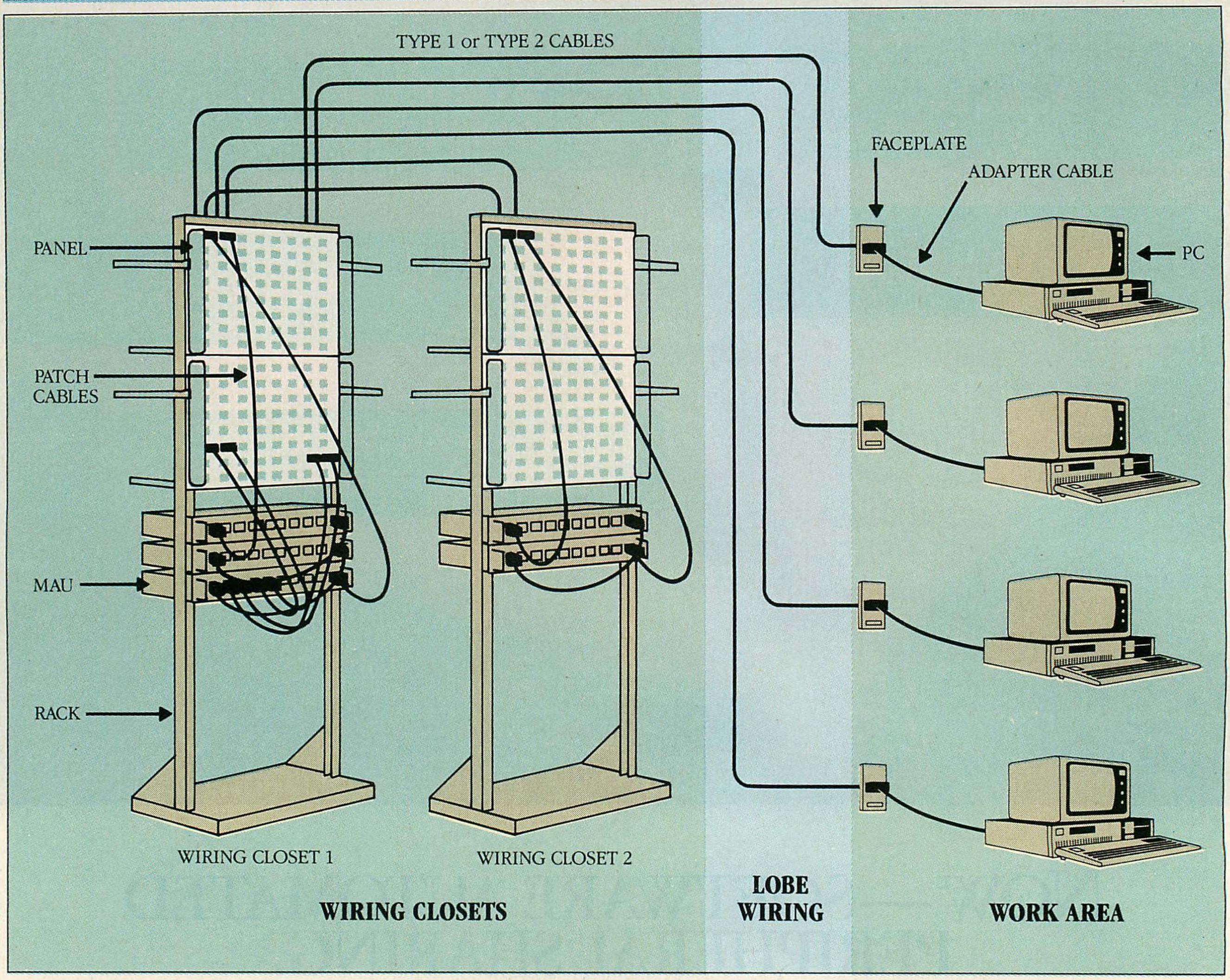
FIGURE 3: *A Complete Cabling System Example*



The wiring closet contains the distribution panel with the MAUs and patch cables providing the link between the various lobes.

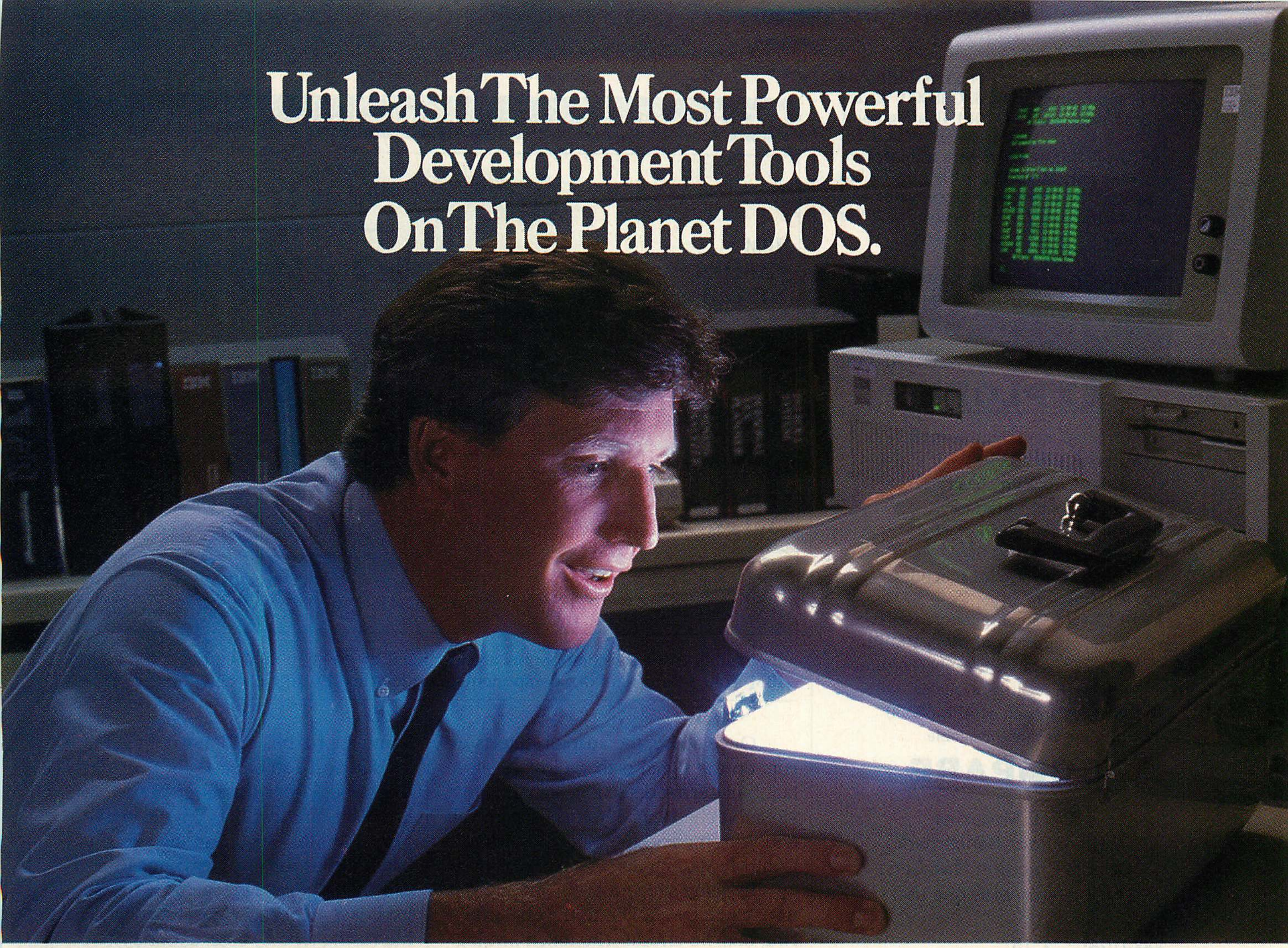
er cable if it is within 150 meters of the MAU. If the MAU is rack-mounted in a wiring closet, as shown in figure 3, then a patch panel is needed to jumper from type-1 or -2 cable (originating at the work area and terminating at a rack panel) to type 6. (Recall that if type-3 wire is used from the work area to the wiring closet, a special filter jumper is required to patch from a punch-down block to a panel or MAU.)

Part of the network/cabling planning process is to identify (and label) all components in the cabling system; a set of charts or tables should be kept that identify various components. Figure 4 shows a sample labeling scheme, as recommended by IBM. Cabling components are identified by an eight-digit number: a four-digit location code, the rack number, the panel number, and a two-digit *x-y* rack coordinate. IBM Token-Ring components are identified by an eleven-digit number: the first five digits are the same as the cabling scheme; digits six through nine indicate the unit number; the last two digits identify the receptacle. Implementing these labeling procedures in the planning process and throughout the installation can help ensure an uncomplicated maintenance of the system.

CONNECTING THE TOKEN-RING

The IBM PC is connected to the Token-Ring by supplying a type-6 adapter cable (available from IBM) with a cabling system data connector at one end and an industry-standard DB-9 connector at the other (pins 1 and 6 are receive, 5 and 9 transmit—the shield is connected to the metal shell). This cable attaches to the back of the IBM PC Token-Ring Adapter I or II (which will be discussed in the subsequent article). For type 3, a different adapter cable (not available from IBM) is used that has the DB-9 connector at one end with a built-in filter housed in its shell, and a 6-pin modular plug at the other.

Internal diagnostics in the IBM PC Token-Ring Adapters test the internal circuitry, ring interface drivers and receivers, and external cable and lobe wiring. To insert itself into the ring, the internal diagnostics goes through five phases. In the first phase, the lobe wiring to and from the MAU are checked via a wrap mode. The second phase involves activating the phantom DC signal to drive the relay at the MAU, then waiting for an active ring monitor frame. If one is not detected, that PC becomes an active monitor. The third phase serves to make certain that a duplicate address does not exist on the ring. The fourth phase is neighbor notification, in which all adapters become aware of their upstream neighboring adapter's address. In the final phase, to become active, the diagnostics request parameters in the passing of tokens and frames.



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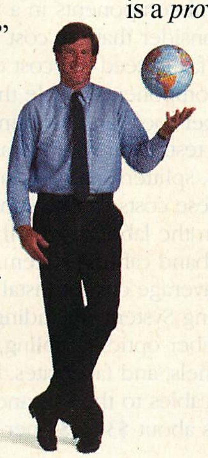

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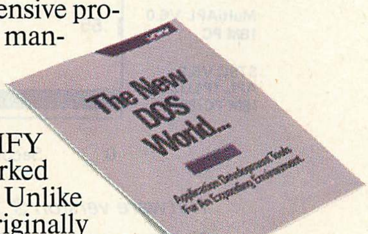

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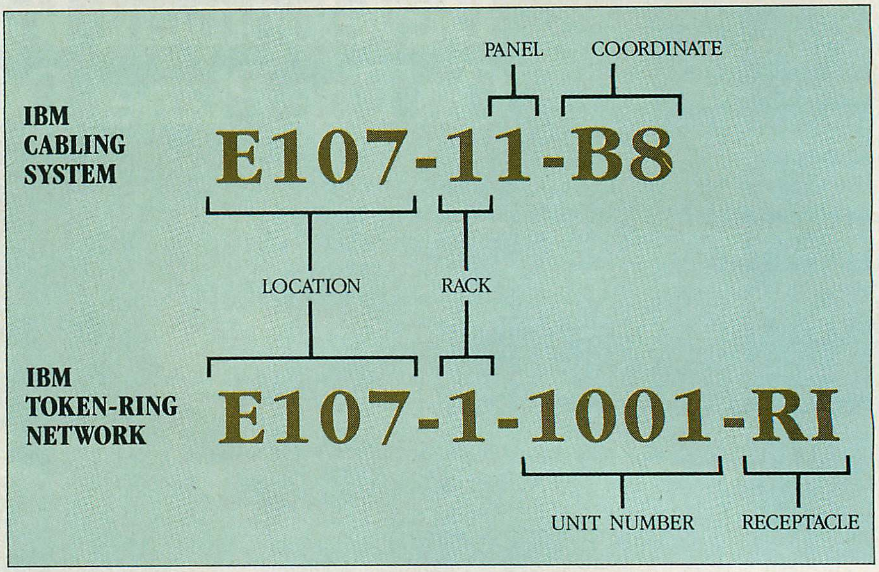
FIGURE 4: *Component Labeling System*



IBM Cabling System components are identified by an eight-digit number (top). The IBM Token-Ring Network components are identified by an eleven-digit number.

Adapted from IBM Token-Ring Network Introduction and Planning Guide

Once active, the adapter detects errors on the signal path via loss of signal, burst error detection, signal code violation checking, 32-bit checksum validation in frames, and Media Access Control (MAC) frame checking.

In some situations, the amount of time taken by a token to traverse the ring may be critical. The token-passing time is a function of the interface delay plus propagation delay in the wire. The interface delay is less than 2 bits per adapter, plus 24 bits for the active monitor station (which must buffer 24 bits to ensure that the ring can pass the minimum number of bits—the three-byte token—in a single circulation). Propagation delay in copper wire is about 5 microseconds per kilometer, which yields a delay of approximately 1 bit per 1,600 feet in a 4-Mbps ring.

COST CONCERNS

In the process of calculating the cost of the physical components in a wiring system, consider that the cost of labor often can far exceed the cost of the physical components. Cable that costs 20 cents per foot can cost hundreds of dollars to test. Even when head-ends, amplifiers, splitters, and so on, are added in, these costs can be substantially lower than the labor to install and test the broadband cabling system.

The average cost of installing the IBM Cabling System (including copper—no fiber optics—cabling, MAUs, wiring panels, and faceplates, but not the drop cables to the PCs and no repeaters) is about $3 to $4 per foot. Some approximate IBM pricing is as follows: type-1 cable retails for $.40 per foot, type-5 fiber for about $3 per foot; faceplates are less than $3; the eight-port IBM MAU $660; and eight-foot patch cables for use in wiring closets can be had for $34. Type-6 cabling by itself is $.45 per foot; the PC adapter cable (using type 6) costs about $35.

Installation of a cabling system involves four basic steps: planning, ordering, installing, and testing. To plan cabling for a token-ring requires understanding all of the components of the system. Cable choice will be largely dictated by building codes and whether or not the cable will accommodate voice (telephone) service in addition to Token-Ring data. Voice service accommodation also will dictate which faceplates are selected for the user work area.

If outdoor type-1 wire is employed, IBM strongly recommends the use of surge suppressors to guard against damage from voltage surges. Caution must be exercised because of the possibility of an excessive ground potential difference between two power services' grounding systems. This could become a hazard between two buildings that are powered by different service entrances (multiple transformers); it also could occur in a very large facility.

The work area is a good place to begin planning. A survey of the types and quantities of PCs will help to determine the accessories needed. The work area location will determine the cable type, version (plenum, nonplenum, or outdoor) and length (distance from the

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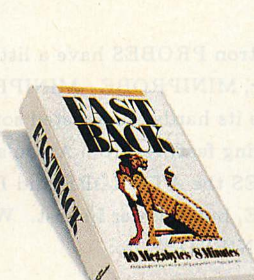

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wiring closet) needed. Cable choice will determine the support system needed. For type 3, extra care must be taken to avoid intercoms, fluorescent lighting, power cables, arc welding equipment, heating equipment, electric motors, or any high-voltage equipment.

Concurrently with determination of work area requirements, potential wiring center sites should be identified. Trade-offs can be made between one or two large centralized wiring centers or several smaller, decentralized centers. While the choice of fewer wiring centers can mean easier maintenance of the cable, it also may require larger amounts of cable. If the system is small, wiring closets may not be necessary. A system could be made up of a couple of MAUs with patch cables.

With the exception of the actual wire, components can be ordered through IBM or a third-party independent contractor. Many third-party contractors also offer site survey and planning services. All ROLM parties are authorized cable installers (ROLM is a wholly owned IBM subsidiary).

Wire installation probably will be the most time-consuming task in the process. Factors that will affect installation time and cost include accessibility of the work area and path back to the wiring center, whether the installation must be done by union personnel, and the time spent stripping wires, crimping connectors, and so on.

Once the cable is installed, testing should be performed before any devices are connected. IBM produces a cabling system tester that detects faults in copper data and telephone wiring by measuring continuity in the cabling system. For fiber optics (type-5 cable), a separate tester is available.

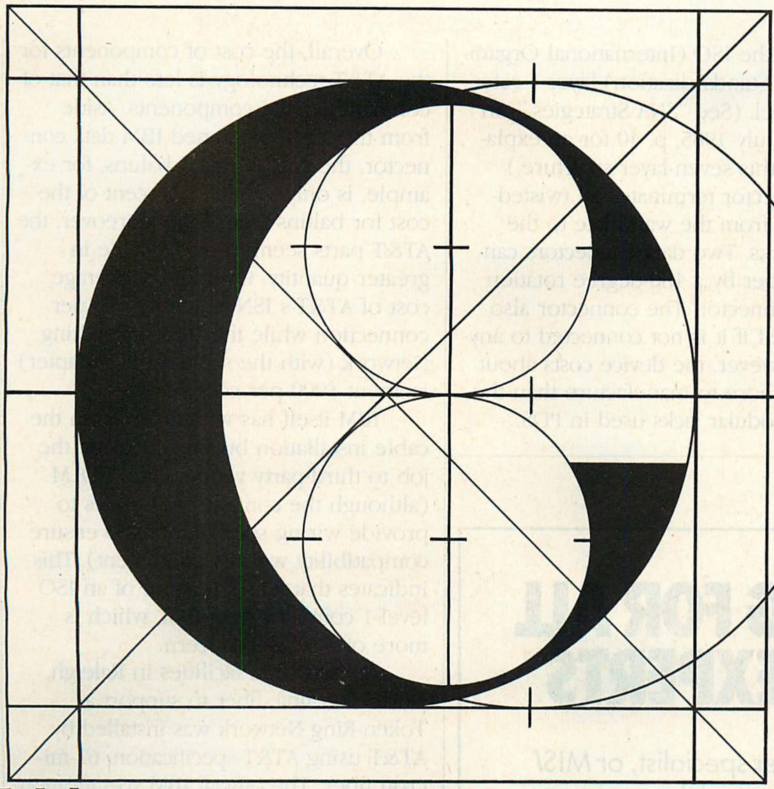
Managing the cabling system involves the assignment of MAU ports to PCs (while ensuring that the cabling plant remains operational) and developing the system as PCs are added or moved. Not all work areas can be predetermined and prewired.

A good system design will facilitate testing in the event a component should fail. In the case of a single wiring closet, the manager can create a test ring consisting of a single MAU. MAUs are added to the test ring until the ring fails, thus identifying the failed MAU. In the case of multiple wiring closets, the wiring closets can be isolated from each other, followed by isolation of the MAUs within each closet. The ring test is performed while connecting the MAUs one at a time, then they are connected to another wiring closet and its MAUs, until the offending MAU is isolated. Further resolution is provided by unplugging the lobe wiring from the MAU that connects a certain PC.

FUTURE CONNECTIONS

As noted, AT&T's PDS is an alternative to the IBM Cabling System. PDS is a multifunctional distribution system that supports voice, data, graphics, and video communications on premises. It uses fiber-optic and twisted-pair media and is suitable for single-building, multitenant, high-rise, or campus environments. PDS supports all AT&T products (such as the ISN and STARLAN networks), as well as other vendors' products. (For example, with the use of adapters and the AT&T Premises Lightwave System, PDS supports IBM 3270 terminals).

PDS consists of six distribution subsystems and a grouping of equipment: campus, backbone (riser), horizontal wiring, work location wiring, equipment wiring, and administration. It is based on an AT&T model that allows a distribution system to be divided into subsystems that can be individually



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designed according to user needs, communication system requirements, and building topology. This approach also facilitates logical and economical distribution system upgrades. The IBM Cabling System is similar in concept, but its overall view currently is not as well developed as that of AT&T.

One interesting aspect of the IBM Cabling System was the introduction of a new data connector, one referenced in an appendix to the IEEE 802.5 MAC standard. Technically speaking, cables and connectors usually are not defined as part of the ISO (International Organization for Standardization) layer-1 reference model. (See "SNA Strategies," Art Krumrey, July 1985, p. 40 for an explanation of this seven-layer structure.) This connector terminates all twisted-pair wire, from the wall plate to the wiring racks. Two data connectors can join together by a 180-degree rotation of one connector. The connector also shorts itself if it is not connected to anything. However, the device costs about 20 times more to manufacture than the RJ-style modular jacks used in PDS.

Overall, the cost of components for the AT&T technology is less than that of comparable IBM components. Aside from the aforementioned IBM data connector, the cost of AT&T baluns, for example, is only about 75 percent of the cost for baluns from IBM. Moreover, the AT&T parts seem to be available in greater quantity. Overall, the average cost of AT&T's ISN is about $400 per connection while the IBM Token-Ring Network (with the standard PC Adapter) is about $900 per connection.

IBM itself has withdrawn from the cable installation business, leaving the job to third-party vendors and ROLM (although the company continues to provide wiring specifications to ensure compatibility with its equipment). This indicates that AT&T is more of an ISO level-1 company than IBM, which is more of a level-7 concern.

At three IBM facilities in Raleigh, North Carolina, fiber to support a Token-Ring Network was installed by AT&T using AT&T-specification, 62-micron fiber. The official IBM specification calls for 100-micron fiber; however, the new IBM Token-Ring Network Optical Fiber Cable Options documentation describes how to use non-100-micron fiber and what the limitations are. Perhaps this is the first step toward AT&T PDS/IBM Cabling System integration or even an ISN/Token-Ring merger.

Another IBM Cabling System enhancement seems imminent. Nearly every IBM paper contributed to a publication or conference that discusses the Token-Ring mentions additional (but as yet unavailable) Token-Ring requirements. One such item appears to be a device similar to 3Com's RingTap MAU: in one paper ("The IBM Token-Ring Network Technology, IBM), the company mentions the "fan-out connector," which can be used to expand an MAU tap. This connector does not replace the MAU, but can be used to expand an area in which only a single data tap exists and more devices must be added to that tap. This connector would ensure that the phantom signal required to drive the MAU relay would come from only one active station and that turning stations (connected to the fan-out connectors) on and off would not be disruptive to the MAU relay.

What does IBM hold for the future? Greater variety in host attachment, as evidenced by the trend in its announcements for the indirect connectivity of larger hosts to the Token-Ring from the original PC base; a 16-Mbps bandwidth for graphics; file transfer; backbone rings; and processor-to-processor (dis-

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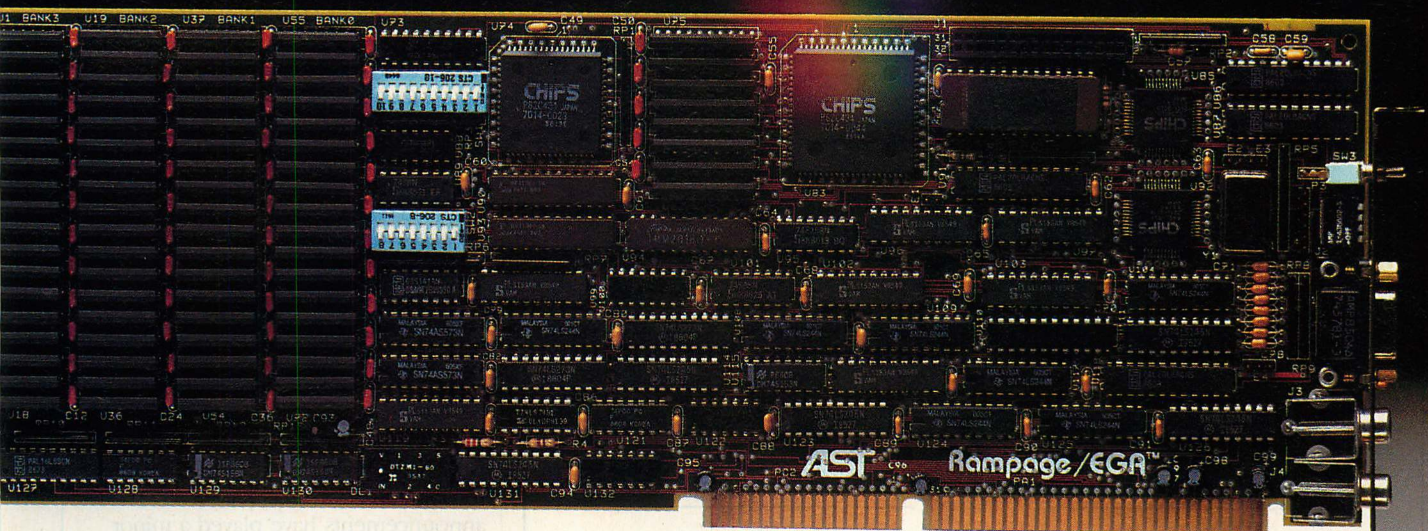

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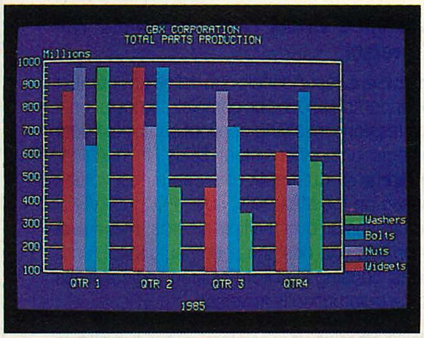

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tributed) applications. The estimate of 16 Mbps as the logical bandwidth increase developed both from the need for a bandwidth greater than 4 Mbps and from the fact that IBM test results on types 1 and 2 show that the cable is satisfactory up to that speed.

Also likely is additional network management of performance, configuration, operations, and authorization. This is indicated by the announcement of NetView/PC, and by the added requirements for the Token-Ring in IBM literature, which show a single point of control for interconnected rings. Gateways to X.25 packet networks probably will begin to appear as the X.25 protocol becomes supported on larger hosts. ISDN, non-IBM LANs, and remote LANs also are likely to be supported; however, a direct connection to the ROLM CBX does not seem to be a short-term priority in terms of Token-Ring product development. As evidenced in the IBM literature, the migration path for ROLM CBX users is to interface the ROLM CBX through an asynchronous server. (ROLM announcements have played a minor role thus far in the unfolding of the Token-Ring, but users eventually might expect to see a direct connection between the two systems.)

IBM has devoted many pages to the key components and aspects of the cabling system discussed here. Recommended publications from IBM include: *IBM Cabling System Planning and Installation Guide* (GA27-3361), *IBM Token-Ring Network Introduction and Planning Guide* (GA27-3677), *IBM Token-Ring Network Telephone Twisted-Pair Media Guide* (GA27-3714), and *IBM Token-Ring Network Optical Fiber Cable Options* (GA27-3747). These publications are available from IBM Distribution Center (717/691-2000). The components for the Token-Ring can be purchased from any authorized IBM supplier. A few of the larger suppliers are Anixter Brothers (Skokie, Illinois), John B. Rudy Company (Long Beach, California), and AMP, Inc. (which refers inquiries to a local distributor), and General Electric. All ROLM distributors and installers are authorized as well.

As the IBM Token-Ring system comes into better focus, users who have taken an early look at their cabling and work area needs will be in the best position to put the power of this advanced network technology to use.

J. Scott Haugdahl is a senior systems specialist at Architecture Technology Corporation, a Minneapolis-based consulting, publications, and seminar firm for data communications.

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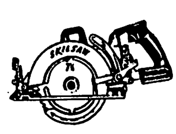

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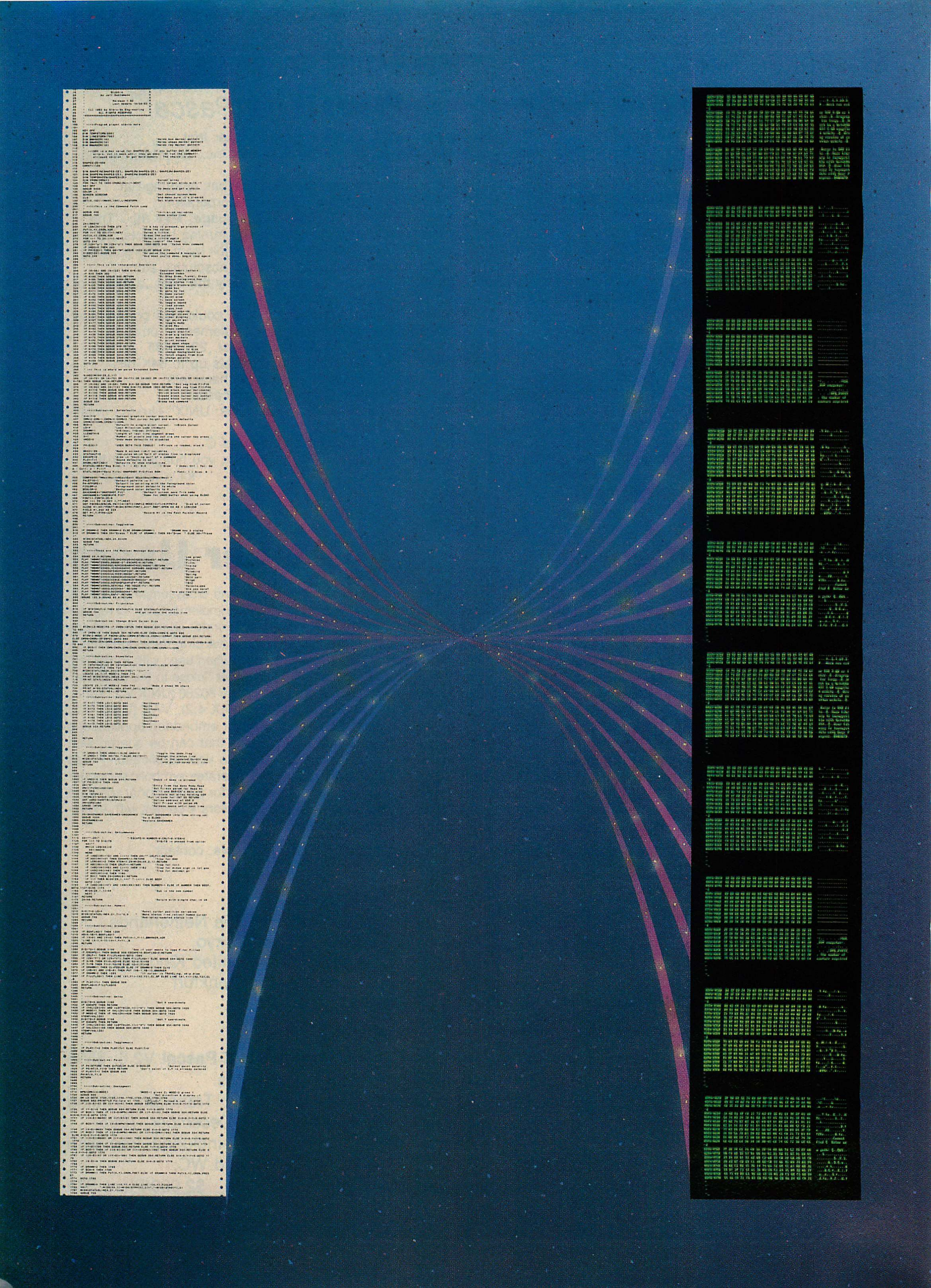

Reconsidering BASIC

The current group of BASIC compilers are improved enough to earn renewed respect among professional programmers.

MARTY FRANZ

Traditionally, BASIC compilers have suffered from a lack of respect. Faced with using a language that lacks block structures, definable data types, and sophisticated graphics, professional software developers have rejected BASIC out of hand and turned to C, Pascal, or Modula-2 to write their applications. Novice programmers considered BASIC compilers too difficult to use for running simple programs. Caught between an archaic language definition and serious ease-of-use problems, the few BASIC compilers available for the IBM PC have been a tool of last resort, a way to speed up or compress a large interpreted program.

That situation, however, is changing. Several versions of BASIC have been announced for the PC, many of which are good enough to make serious programmers once again consider BASIC. Five compilers (all but one including an editor and programming environment) are examined here. Though varying widely in features, BASICA compatibility, and price, all are competent compilers. (BASIC interpreters were reviewed in "Six New Shapes of BASIC," Ted Mirecki, June 1986, p. 52.)

The compilers reviewed here are: IBM BASIC Compiler 2.0, Microsoft's QuickBASIC 2.0, Pecan Software System's (formerly UCSD) BASIC 4.4, Softaid's MTBASIC, version 2.6g, and Zedcor's ZBasic 3.0. All of these products are classed as compilers because they can produce stand-alone executable object files (either .COM, .EXE, or, in the case of Pecan BASIC, .CODE).

Each of the compilers was evaluated using the following criteria:

Function. Does the compiler include enough of the BASIC language with which to write concise programs? Does it have extensions for structured programming, graphics, and sound?

Transparency. If a standard exists for BASIC on the PC, it is the BASICA interpreter included as part of DOS. Numerous commercial programs have been written in this dialect of BASIC. Does the compiler make conversion from BASICA easy? What restrictions are enforced on the user?

Ease of use. Is the compiler a DOS command invoked batch-fashion or a complete environment for programming? What amenities are offered to the programmer in the environment?

Documentation. Even though BASIC is a widely known language, subtle differences exist between compiled and interpreted implementations. Are these adequately explained in the documentation? Does the manual provide enough information for linking in assembly language or other object files? If the inter-

ILLUSTRATION • BOB PASTERNACK

preted BASIC is extended in implementing the compiler, are these additions adequately described?

Performance. How fast and small is the generated code? Does it run as a .EXE or .COM file? (.COM files have a 64KB size restriction.) Does it generate well-behaved programs? To help evaluate execution speed and code size, the benchmarks used in the June 1986 review of BASIC interpreters are repeated for the compilers. In addition, compilation times are measured, because this is a significant consideration in using a compiler instead of an interpreter.

EXTENDED FEATURES

The features of the reviewed compilers are summarized in table 1. They all have extended interpreted BASIC beyond its confining line orientation—by adding block structures (such as a LONG IF, where multiple statements can be used), making line numbers optional, or allowing defined functions to span more than one line. The IBM BASIC Compiler and Microsoft's QuickBASIC allow for separately compiled subroutines to use their own local variables. Despite these improvements, none of the compilers implements the ANSI standard in these areas (see "The ANSI Standard for BASIC," Jim Harle, June 1986, p. 72) and, in fact, only IBM BASIC and QuickBASIC are fully compatible with interpreted BASICA.

Four of the five compilers include some form of development environment in addition to the translation of BASIC from source to executable object code. The environment usually consists of a coresident editor and compiler, making it unnecessary to quit the editor in order to compile a program.

IBM. IBM was one of the first vendors to release a BASIC compiler for the PC. Its version 1.0 BASIC Compiler was developed by Microsoft and released in 1982. This initial version, though offering a great performance improvement over interpreted BASICA, had a number of bugs and limitations. A set of seven patches was needed to make the compiler work properly. Further, the memory model of version 1.0 restricted the programmer to 64KB of compiled code and 64KB of data (small model), which limited the product's usefulness.

The IBM BASIC Compiler 2.0 is a welcome improvement. Besides cleaning up the bugs, this new version is more powerful than 1.0. Programs written with version 2.0 can use all of available memory (large model) and can create large dynamic arrays. Many extensions to BASICA are supported, including labels, long function definitions, and separate subroutines with their own sets of variables. Even with these extensions, the compiler is highly compatible with the BASICA interpreter; the biggest exception is the stipulation that statements such as DIM and COMMON must precede references to their defined storage in the order in which lines are compiled as well as the order in which they are executed.

These exceptions are thoroughly explained. Documentation, which was skimpy in the original version, has been

TABLE 1: *Compiler Features*

	IBM	MICROSOFT	PECAN	SOFTAID	ZEDCOR
Model	BASIC 2.0	QuickBASIC 2.0	Pecan BASIC 4.4	MTBASIC 2.6g	ZBasic 3.0
Price	$539.00	$99.00	$79.95	$49.95	$89.95
BASIC FEATURES					
Recommended memory (KB)	128	256	128	128	128
DOS 2.x, 3.x path support	●	●	○	○	●
BASICA compatible	●	●	○	○	○
Separate compilation	●	●	●	○	●
.OBJ output	●	●	○	○	○
.EXE output	●	●	○	○	○
.COM output	○	○	○	●	●
User configurable	○	●	●	○	●
Not copy protected	●	●	●	●	●
PROGRAMMING ENVIRONMENT					
Development environment	○	●	●	●	●
Editor	○	●	●	●	●
Full screen	○	●	●	○	○
Block commands	○	●	●	○	○
Mouse support	○	●	○	○	●
Microsoft Windows support	○	○	○	○	○
LANGUAGE EXTENSIONS					
Optional line numbers	●	●	●	○	●
Labels	●	●	○	○	●
Long functions	●	●	●	●	●
Subroutines	●	●	●	○	●
Long IF	○	●	○	○	●
Block structures	●	●	○	○	●
Record structures	○	○	○	○	○
ISAM	●	○	○	○	○
Dynamic arrays	●	●	●	○	○
BCD math	○	●	○	●	○
Multitasking	○	○	[a]	●	○
ANSI standard	○	○	○	○	○
HARDWARE SUPPORT					
8087 math	○	○	●	[b]	○
Mouse calls	●	○	○	●	○
Light pen	●	○	○	○	○
Graphics	●	●	○	○	●
Support of other operating system hardware	○	○	●	●	●

● = *Yes* ○ = *No*

[a]*Concurrent routines written in p-System Pascal may be linked to nonconcurrent Pecan BASIC code.*
[b]*The 8087 version of MTBASIC is available for $79.95.*

Though they start with the same language (the so-called Dartmouth version of BASIC) the various types of extensions make each of these compilers unique.

expanded to two manuals: one that describes the use of the compiler and a language reference manual. Both are well-indexed and complete.

Of the five compilers reviewed here, IBM's is the only one limited to operating from the DOS command line instead of through an integrated development environment. A single module, BASCOM20.EXE, reads an ASCII source version of the BASIC program and produces an .OBJ file, which must then be linked with supplied libraries to produce a .EXE file. The program may be linked either to run stand-alone or to use a resident runtime module called BASRUN20.EXE, which is loaded separately and maintained in memory when the program is run. If the separate runtime module is used, overlay chaining is possible with the CHAIN statement. The runtime module, however, must be licensed through IBM if it is to be distributed with commercial software.

Within the source program, directives can be issued to the compiler with specially formatted comment statements. These directives can produce paginated listings and include library source files. Along with the directives, a myriad of command-line switches are provided to control compilation. Some, such as those controlling event trapping and communications, are sure to confuse inexperienced programmers. Omitting a necessary switch (such as not enabling error trapping in a program using ON ERROR) produces a diagnostic message and requires recompilation with the correct switch.

This traditional edit/compile/link method of operation has two advantages: first, the process of creating executable BASIC programs from large and complicated series of source files can be automated by using batch commands; second, third-party object modules written for use with IBM compiled BASIC programs can be linked into the final .EXE file. Unfortunately, the high-level language integration that Microsoft has built into its C, Pascal, and FORTRAN products (see "Language Integration," Product of the Month, Jeff Duntemann, July 1986, p. 29) does not extend to compiled BASIC, and subprograms written in those languages cannot be linked to BASIC. Routines written to certain requirements in Microsoft MASM 4.0 can, however, be incorporated into IBM compiled BASIC.

A unique feature of the IBM BASIC Compiler is the inclusion of an indexed sequential access method (ISAM) that allows data in files to be retrieved and updated using an alphanumeric *key* field instead of a record number. Previously, programmers who needed this capability from BASIC had to purchase third-party libraries. IBM's ISAM is implemented as a separate, resident module called ISAM.EXE, which is loaded into memory ahead of any compiled BASIC program. Calls are made from a compiled BASIC program into this module, which performs ISAM functions on behalf of the requesting program.

Unfortunately, no improved data structuring method is available to go along with this access method; BASICA's cumbersome FIELD statement must be used to define data records. While mainframe programmers should have no trouble using IBM's ISAM, PC BASIC programmers may find the documentation and concepts a bit foreign. Nonetheless, like a sort package, a functional ISAM is an important facility for business programmers to have.

Microsoft. Although version 1.0 of Microsoft's QuickBASIC was an uninspired repeat of the IBM BASIC Compiler 1.0, version 2.0 is a substantial and exciting improvement. More than a batch compiler, QuickBASIC 2.0 is an integrated, mouse-driven, windowed development environment. (QuickBASIC 2.0 was named *PC Tech Journal*'s Product of the Month, November 1986, p. 31.)

Like the IBM BASIC Compiler, QuickBASIC has many language extensions, including named subroutines and block structures. It still compiles normal BASICA with a few exceptions (DIM, COMMON). It now has a great deal of flexibility in compilation options. Programs can be optimized for size or speed, compiled to memory for immediate execution, and compiled with the inclusion of debugging information. These options are much easier to use than IBM's compiler because they are set from a single control panel displayed when a program is compiled instead of with the inconvenient switches IBM uses. Once the options are selected, the environment remembers them for future use. This makes compilation extremely fast and easy.

A Macintosh-style, full-screen editor is supplied as part of the QuickBASIC development environment. Remarkably, this editor is implemented in text mode, but clever use of the PC's special characters in displaying pull-down menus and windows gives the QuickBASIC editor the feel of graphics-oriented editors. Its mouse-driven cut and paste features work well, and it has a sensible (but not fancy) set of options. For those who insist, the QuickBASIC compiler also can be run batch-style.

At runtime, QuickBASIC programs have essentially the same structure as IBM BASIC programs, with a separate runtime module required to support chaining and data sharing among different modules. Compilation options can be selected to generate the object program to disk or to memory with automatic linking and execution, so the complete compile/link/run process can be accomplished in one step.

An important capability in QuickBASIC that is lacking in other BASIC compilers is the inclusion of a debugger and animator in the development environment. With them, the programmer can run a program in slow motion, stopping when necessary to change variables. QuickBASIC also is the only compiler tested that supports IBM's Enhanced Graphics Adapter in 640-by-350 color graphics modes.

Another feature of QuickBASIC that the other reviewed compilers do not have is that QuickBASIC easily allows a programmer to create and use libraries of compiled BASIC subprograms. User libraries are actually compiled QuickBASIC subroutines that are bound by the BUILDLIB utility into a USERLIB.EXE file that is loaded at start-up time, a very difficult task in an interpreted BASIC environment. Commonly used subprograms (such as screen I/O routines, report writers, database access) now can be written, compiled, and easily reused in countless programs. No third-party commercial libraries exist at this time, but that is likely to change.

QuickBASIC is not truly compatible with any of Microsoft's other BASIC implementations for non-IBM or compatible machines. It also does not implement any of the proposed ANSI standard for BASIC. Further, despite many conceptual similarities, QuickBASIC is not compatible with Microsoft Windows; without interfacing to assembly language, Windows services cannot be accessed from a QuickBASIC program. Because Windows is widely reported to be one of Microsoft's key products, this functional omission is a mystery. As a further annoyance, only a Microsoft-compatible mouse is supported by the QuickBASIC environment, although most current mice have a Microsoft-compatible mode. Without the mouse, the environment is not as fluid, but it still works correctly.

These problems are minor when compared to the strengths of QuickBASIC. On the whole, QuickBASIC is an efficient and carefully thought out BASIC development environment for the PC. With its fast in-memory compila-

tion and debugging facilities, QuickBASIC combines the best features of both a compiler and interpreter.

Pecan Software Systems. Like QuickBASIC, the Pecan BASIC compiler is a complete program development environment. The compiler is based on the p-System, which has been in use since 1978 when it was a public-domain development system that was created by the University of California at San Diego (UCSD). The system is founded on the concept of a p-interpreter, a small virtual machine that can be implemented rapidly on a variety of hardware systems. The rest of the development system, written to run on the p-machine, is therefore highly portable. The p-System has been ported to a variety of microcomputers. The development system consists of an editor, compiler, filer (file utility), librarian, and other ancillary programs. The p-System is stand-alone and once it is entered from DOS, the programmer does not need to return to DOS.

The Pecan BASIC compiler runs under the p-machine, as do other p-System utilities and languages. Although the p-System has adequate development facilities, it still represents 1978 conventions for disk management and user interface. In place of DOS's commands and newer-generation editing tools, the Pecan BASIC compiler uses a consistent set of single-character option menus. The system's editor is awkward and complicated, especially when compared to the QuickBASIC editor. At least the options and programs are consistent in their operation, so navigation of the system is straightforward. A DOS filer utility is included to allow files to be transferred to and from DOS and to allow single, large DOS files to be used as p-System virtual volumes for file storage. Further, Pecan BASIC has a DOS bridge feature that allows ordinary DOS disk files to be opened and manipulated from within the p-System.

Documentation from Pecan consists of one thick paperback manual that gives a complete, if somewhat poorly organized, description of the p-System, plus a separate set of loose-leaf pages addressing the BASIC compiler. The BASIC manual contains little more than language reference information. Example programs, especially in the important area of file I/O, are missing. The documentation lacks tutorial information. A disk contains information to supplement and correct the manual.

Installation instructions given in the manual differ significantly from the correct set of instructions obscurely provided in the README file stored on a p-System virtual volume rather than in the DOS disk file as might be expected. The installation process itself involves using the Library function to copy object modules needed by the BASIC compiler into the system object library, plus renaming the BASIC compiler program to be the current system compiler. Both of these steps require backtracking when the system's virtual volumes fill up and are needlessly complicated.

The initial installation of Pecan BASIC during testing for this review would not function with a Hercules-compatible graphics board; replacing it with the IBM Color Graphics Adapter (CGA) resolved that difficulty.

Pecan BASIC is only slightly compatible with IBM BASICA. Programmers writing pure, bare-bones BASIC programs might scrape by, but more complex programs would require extensive conversion. One aggravating quirk is that the PRINT statement, which in every other BASIC implementation directs output to the screen, instead sends output to the printer in Pecan BASIC; the DISPLAY statement must be used in its place. No graphics or sound commands are available, although Pascal modules with these facilities can be linked into BASIC programs. Pascal is the only language that uses the p-System's concurrency capability directly.

Pecan BASIC allows for FORTRAN-style optional line numbers, long function declarations, and subroutines with local variables. It also has a largely undocumented virtual array feature in which very large arrays can be placed in a random-access file and therefore overflow RAM memory. In short, Pecan BASIC is reminiscent of BASIC on large time-sharing systems.

The strongest feature of Pecan BASIC is that it is object-code-compatible across all machines that run on the p-System. Furthermore, output from the BASIC compiler can be linked with other p-System language object modules (Pascal and FORTRAN). Each implementation of the p-System includes a program for sending files across RS-232 links. This emphasis on true portability, facilitating transfer of files between media-incompatible machines, makes Pecan BASIC worth investigating by vertical market developers who do not mind a nonstandard environment if the benefit is reaching as wide a variety of machines as possible with a single version of their product.

Softaid. MTBASIC from Softaid is unique among the BASIC compilers reviewed here in that it implements multitasking. In an MTBASIC program, nine separate

tasks may execute concurrently, performing terminal I/O through separate screen windows. Besides this multitasking capability, MTBASIC offers no extended features—no colors, graphics, sound, or record I/O. This makes MTBASIC a niche product with applications in lab and process control.

A task is initiated in MTBASIC with the TASK and EXIT statements. Each task can be set to run periodically by dispatching it with the RUN statement (not the same RUN as that used to start BASIC program execution), with the period interval specified in PC timer ticks. The task then runs every time the specified number of timer ticks has elapsed. All tasks share the program's variables and are analogous to asynchronous subroutines (that is, subroutines of the GOSUB...RETURN variety).

To complement the multitasking facilities, MTBASIC contains some unusual features. An interrupt address can be assigned to a particular task so that the task is executed when the matching interrupt occurs. In-line machine language may be coded as part of a task, although no assembly language facilities are provided in MTBASIC; instead, a string of hexadecimal machine codes is placed in a statement after the CODE key word. Port I/O is available for direct control applications, and interrupts can be switched off during time-critical processing.

MTBASIC's limited programming environment is reminiscent of the first BASIC implementations for the early Altair and IMSAI computers: statement renumbering is not possible; loading ASCII statements containing embedded tab characters triggers a syntax error; system clock facilities are not available, so times for the benchmarks run for this article were obtained by attaching a timer task that counted ticks elapsed during the execution of the program; no extended DOS directory or path support is included. These limitations are explained in the Softaid manual.

Compilation is done with either the COMPILE or DISK COMPILE command, depending on where the source code is located. No other options are necessary or available.

The weakest part of the MTBASIC package is the documentation, which consists of a slim manual with no index. The differences between MTBASIC and BASICA are not summarized anywhere. More technical information, especially in the areas of multitasking performance and limitations, is a must for the type of programmer who will use this package. On MS-DOS, MTBASIC re-

quires that ANSI.SYS be installed. A CP/M version also is available.

MTBASIC is designed to provide multitasking capability to a BASIC programmer in a straightforward, no-frills package. It does this well.

Zedcor. At first glance, ZBasic from Zedcor looks like a flashy, compact BASIC styled after Borland's Turbo Pascal. Beyond normal BASIC statements and functions, ZBasic also supports device-independent graphics and many extensions. Block structures, such as LONG IF and DO REPEAT, and multiline function definitions are provided. Powerful screen input statements have been added that include the ability to position the cursor and control the length of the entered field. No true business programming facilities such as ISAM or record structures are available. The manual provides good documentation with a sensible organization for programmers who already know BASIC.

The development environment with ZBasic consists of a line-oriented editor with some extensions. It cannot be called a full-screen editor because the cursor cannot be moved with the arrow keys, nor a line edited just by pressing Enter, as in BASICA. Code can be saved in both ASCII and tokenized formats, with or without line numbers. ZBasic also provides indented listings with or without line numbers. However, code cannot be saved back to a file in its indented form for printing with DOS utilities. ZBasic only partially supports DOS paths and directories for files; the CHDIR command must be used, and ZBasic cannot load or save files to or from other directories. Like the language, the environment is portable; the editor key combinations can be used in every version of ZBasic.

Graphics in ZBasic are based on the idea of a virtual device. The screen is considered in all versions to be 768 by 1,024 pixels. ZBasic maps this screen onto the real screen depending on the current screen mode. The aspect ratio of the image stays the same in text and graphics modes—even on different machines. If no graphics mode is available on a given machine, graphics output will be mapped onto the text screen with character positions acting as pixel positions. (The resolution and overall quality deteriorates on text-only or low-resolution displays.) Notably missing in this scheme is BASICA's convenient DRAW statement, as well as the GET and PUT bit-pump statements that allow fast animation. ZBasic does include statements to draw boxes, circles, ellipses, and arcs. Conversion to this coordinate system and these plotting functions from BASICA is cumbersome, but their use in new programs is logical and easy. One nice touch is ZBasic's ability to write to and read from the CGA's extra display adapter memory through the DEF PAGE statement.

In fact, when considering low-level features, ZBasic has several worth mentioning: the program's DOS Ctrl-C address can be trapped and control passed to a ZBasic statement whenever Ctrl-C is pressed; the address of any line in the program can be obtained with the LINE function; a set of jump tables is provided for all of ZBasic's I/O, allowing patching by the programmer for custom hardware.

ZBasic generates .COM files that permit as much as 52KB of compiled code and 64KB of data. Overlays are supported, as are embedded machine-language routines.

The compiler also supports binary-coded decimal (BCD) math, with the precision set when ZBasic is configured. During configuration the user can set default variable types and determine whether direct screen or BIOS I/O is used. Once ZBasic has been configured, the compiler can be saved in its configuration. This allows the programmer to cut down on numeric precision for extra speed or to turn off array-bounds checking as soon as a program is thoroughly debugged and working.

ZBasic is only marginally compatible with IBM BASICA. File I/O and graphics are the potential trouble spots. An optional program is available from Zedcor to help convert from BASICA to ZBasic. This program was used to convert the HAT benchmark (see below). It attempts not only to convert BASICA statements into ZBasic, but also to produce a report specifying areas where further conversion may be needed. The ZBasic program produced by the conversion utility did not run correctly the first time; a syntax error was generated on the LINE statement.

ZBasic suffers from a few idiosyncracies. It places restrictions on string expressions, eliminating the need for reclamation of unused string memory during execution in the compiler; only direct string assignments and single string functions can be used in statements. Embedding key words in variables is forbidden; therefore, longer, more descriptive variable names cannot be used if they contain two-letter keyword combinations such as IF or ON. Console I/O occurs at a low level so

Ctrl-C is not trapped at all times; to enable Ctrl-C trapping, a TRON statement must be added to the program. This allows removal of Ctrl-C trapping for better performance but can cause problems during development.

Tests showed that division by zero is not trapped in any way by ZBasic. Execution does not stop, and meaningless values such as negative infinity are propagated without warning through the real number variables involved in the erroneous expression. Also, all variables assigned values before the execution of a DIM statement are made zero when the statement is executed. Good practice says that all arrays should be dimensioned before the actual work of a program begins, but no warning of this destructive feature is provided in the ZBasic reference manual.

Versions of this BASIC compiler exist for the Apple II, Macintosh, and various CP/M, Kaypro, and Tandy machines. All are documented in a single, paperback manual with individual sections for the differences among versions. All versions are fully portable at the source code level. This claim was verified by the benchmark programs unchanged on the Apple II and Macintosh versions of ZBasic without difficulty. Zedcor offers a $400 developer's package that includes all versions of ZBasic.

BENCHMARK COMPARISON

Because of the wide differences in these BASIC compilers, a single set of benchmarks is, at best, only a rough comparison of their performance in actual programming. The benchmark programs used for evaluation are the same ones used in the June 1986 article, "Six New Shapes of BASIC."

FILEIO reads and writes a 30,000-record file using the FIELD statement and random files. This program tests the compiler's applicability in a business programming environment where large amounts of data are read to or written from files.

The ubiquitous Sieve of Eratosthenes is used for testing integer math and subscripting. It also provides a basis of comparison for programs that are written in other languages.

The HAT program draws a three-dimensional curve using graphics.

The MULDIV program tests double-precision, floating-point math functions, usually a good measure of number-crunching capability.

These benchmarks were run on an IBM PC with DOS 2.11, 512KB of memory, two diskettes, and an IBM CGA. The results are shown in table 2.

TABLE 2: *Benchmarks*

	IBM	MICROSOFT	PECAN		SOFTAID	ZEDCOR
Model	BASIC 2.0	QuickBASIC 2.0	p-Code	Native	MTBASIC 2.6g	ZBASIC 3.0
SIEVE						
Code file size	23,366	27,102	—	—	15,243	13,184
Without runtime module	1,831	3,472	1,024	1,024	—	—
Compile time	128.4	5.2	20.1	20.1	8.9	7.3
Execution time	2.0	2.0	19.0	2.0	10.0	2.0
MULDIV						
Code file size	24,280	28,022	—	—	—	13,184
Without runtime module	1,847	3,472	1,024	1,024	—	—
Compile time	132.3	4.8	18.3	20.1	—	7.3
Execution time	48.0	12.0	34.0	34.0	—	61.0
FILEIO						
Code file size	27,720	31,724	—	—	15,243	13,184
Without runtime module	1,815	3,440	1,024	1,024	—	—
Compile time	141.2	4.3	18.0	20.1	8.9	8.3
Execution time	385.0	263.0	1,584.0	1,769.0	315.0	86.5
HAT						
Code file size	31,260	38,196	—	—	—	14,080
Without runtime module	2,263	3,936	—	—	—	—
Compile time	166.7	6.2	—	—	—	7.4
Execution time	729.0	666.0	—	—	—	7,512.0

All times in seconds; code file sizes given in bytes.

Timings were taken on an IBM PC with 512KB of RAM, dual diskette drives, the IBM Color Graphics Adapter (CGA), and DOS 2.1. Wherever possible, all programs were compiled from disk to disk; only Softaid's MTBASIC required source to be in memory.

IBM's is the only product incapable of compiling to memory, and its timings point up one powerful advantage of a programming environment. Pecan's native code for MULDIV does not help execution speed because virtually all p-System real number support is in a p-code library and is not recompiled as native code.

MTBASIC was unable to run the MULDIV and HAT benchmarks because the compiler does not support double-precision numbers and graphics. A version of MTBASIC incorporating 8087 math support is available from Softaid for $79.95. MT8087 is a complete version of MTBASIC that does not require the presence of the non-8087 version. It does require that an 8087 coprocessor be installed at all times during both development and execution of code.

Pecan Software's compiler was unable to run the HAT graphics benchmark because no graphics statements are directly available to the p-System BASIC programmer.

Microsoft's QuickBASIC programs were run with no debugging support included and the type of compiler optimization set for *speed* for execution times and *size* for module sizes.

The IBM and Microsoft compilers consistently produced the fastest execution times with the curious exception of FILEIO in which MTBASIC and ZBasic turned in faster performances. ZBasic, however, was slow in executing the HAT benchmark because of its conversion from a small 320-by-200 coordinate system to ZBasic's much larger 1,024-by-768 virtual coordinate system.

When considering module size, IBM and Microsoft produced the largest stand-alone modules. The programmer has the option of compiling a module without the runtime code. These modules are extremely small, but require the presence of the runtime library as a separate file on disk in order to run. In a situation in which many compiled modules chain from one to another, this strategy can save a great deal of disk space. The IBM compiler's runtime module is 63KB, and QuickBASIC's is 68KB. The p-System modules for Pecan BASIC are extremely small, but require a separate p-machine interpreter and runtime library to execute. None of the compilers produces excessively large amounts of code that would pose problems to developers.

The Pecan compiler's times were slower than the others, indicating the performance penalty the portable p-machine approach exacts on execution time. The p-System native code generator is quite good, as the improvement in SIEVE performance indicates. Performance in the MULDIV benchmark, however, was not substantially different under the native code generator because most real number support consists of p-code libraries that are called by the native code but are not native code themselves. An 8087 native code generator is included.

Also to be considered when using a compiler is compilation time. In everyday use, a slow compiler robs programmers of productivity by forcing them to wait for their programs to complete. All of the reviewed compilers performed respectably in this area. The entire compilation process (including linking, if any is required) was timed with a stopwatch. All compilers except MTBASIC were set up to compile source code from disk to disk-based object code files. A .BAT file was constructed for IBM BASIC because LINK is needed in order to produce a .EXE file.

Microsoft QuickBASIC is phenomenally fast in compilation. Moreover, once the desired compilation options have been set up, only a single key (F5) is needed to recompile and link the entire program, making the process not only fast but also convenient.

BASIC COMEBACK

Despite some of the problems mentioned for each product, especially in the areas of compatibility and intersystem portability, all of the BASIC compilers reviewed are adequate tools for software developers.

The IBM BASIC Compiler is recommended only to those programmers who must have ISAM and compatibility with previously compiled software. It is often cumbersome to use and is substantially more expensive than any of the other compilers.

Pecan BASIC is a competent product but limited in audience to p-System programmers. By itself, Pecan BASIC does not offer enough functions to induce a programmer to adopt the p-System, which still has a unique niche among PC development tools; it is a truly portable, multilanguage programming environment guaranteed to run on a variety of hardware.

MTBASIC is worth considering for multitasking applications. It is a solid, credible product despite its slim documentation and lack of features.

ZBasic is extremely portable across the most popular microcomputers and has adequate graphics for applications that do not require fast animation. It also includes an impressive number of system access features such as DEF PAGE. Of the compilers reviewed here, ZBasic was the most fun to use. It has a real "personality" and a solid feel, although its limitations make this recommendation conditional. Zedcor provides good support with a user's group, newsletter, and toll-free number.

Microsoft's QuickBASIC outstrips all of the other compilers. The only problems worth mentioning are that it does not interface with Windows in any way (bindings should be built right into the language to work in this important new environment); the environment is somewhat clumsy without a mouse; and it should support the ANSI standard for BASIC or address the real portability needs of Microsoft BASIC programmers. Aside from these quibbles, QuickBASIC is an excellent offering.

IBM BASIC Compiler 2.0: $539.00
IBM
P.O. Box 1328-S
Boca Raton, FL 33432
800/426-2468
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QuickBASIC 2.0: $99.00
Microsoft Corporation
16011 NE 36th Way
Redmond, WA 98073-9717
800/426-9400; 206/882-8080
CIRCLE 347 ON READER SERVICE CARD

Pecan BASIC Compiler 4.4: $79.95
Pecan Software Systems, Inc.
1410 39th Street
Brooklyn, NY 11218
718/851-3100
CIRCLE 348 ON READER SERVICE CARD

MTBASIC 2.6g: $49.95
MT8087: $79.95
Softaid, Inc.
P.O. Box 2412
Columbia, MD 21045
301/964-8455
CIRCLE 349 ON READER SERVICE CARD

ZBasic 3.0: $89.95
Zedcor, Inc.
4500 E. Speedway #22
Tuscon, AZ 85712
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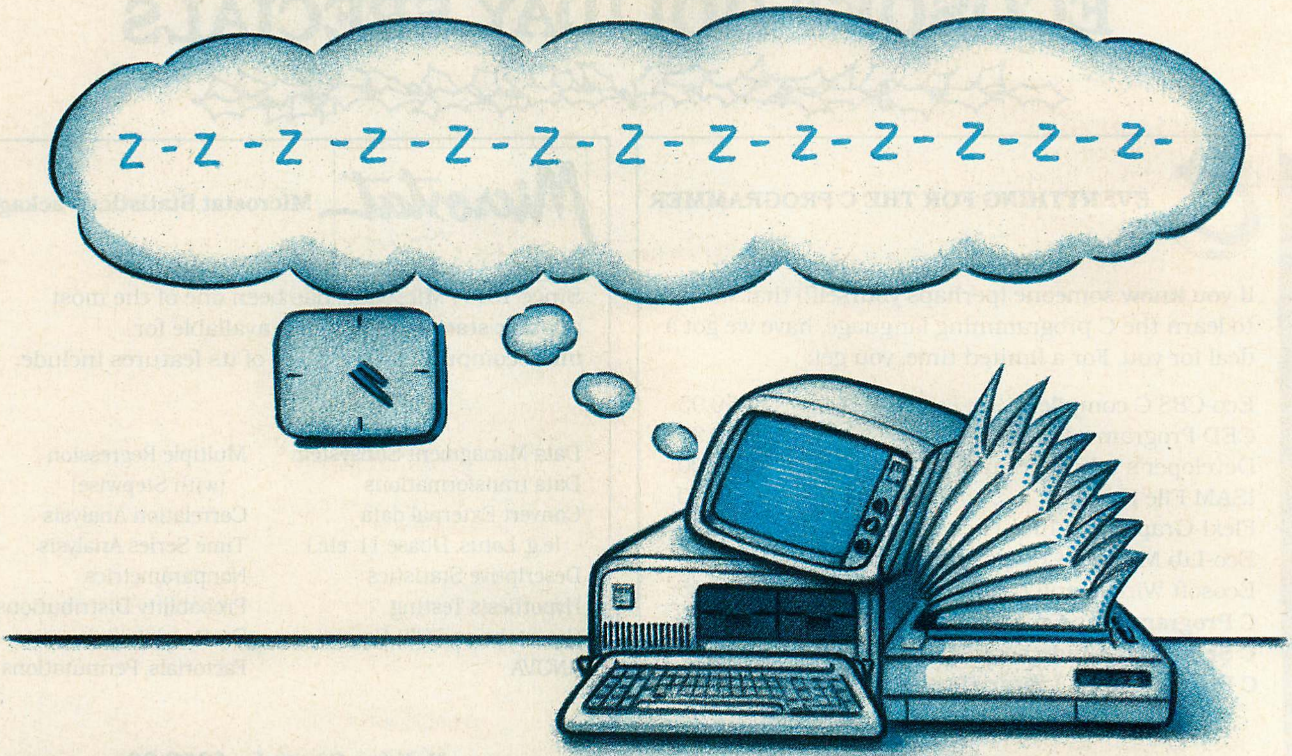

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UNIX™	CODATA	8Mhz 68000	187
XENIX™	ALTOS	5Mhz 8086	96
UNIX™	FORTUNE	6Mhz 68000	95

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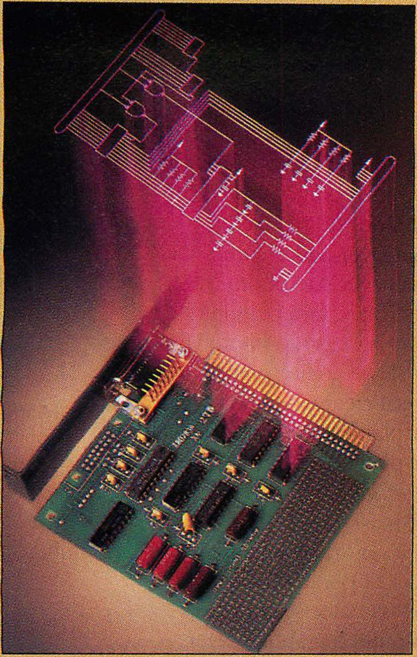

End-to-End Design

Part 2

The layout end of PCB-3 from P-CAD takes the user through to the production of PCB designs, although the course is not as clear as it was at the schematic front end.

RICHARD ANGELL

The essence of any electronic CAD system is its ability to automate printed circuit board (PCB) layout. Some systems provide only the front end—the schematic part of the process; others offer only the layout end. Some packages that include elements of both do so with limitations on flexibility that can render them ineffective. Other products may lack internal integration for data transfer from the front end to the back end, or they may not perform back annotation of schematics.

PCB-3 from Personal CAD Systems, Inc., or P-CAD, provides both. In the November 1986 issue, the schematic portion of the system was reviewed (see "End-to-End Design," Richard Angell, p. 96). The focus here is the second half of the system, PCB design, including PC-CARDS, the interactive editor; PC-PLACE, a placement program; and PC-ROUTE, an autorouter. PC-PHOTO, the utility for producing photo plots, is also examined.

PC-CARDS is similar to PC-CAPS (the schematic editor central to the front-end design). The initial sign-on, first-choice, and configuration screens are nearly identical, as are the main editor menus and status lines. PC-CARDS also operates like PC-CAPS, except that it is not hierarchical. The major difference between the two is that the objects PC-CAPS handles are logical entities called *symbols*, whereas PC-CARDS manipulates *parts*. Table 1, a list of PC-CARDS commands, can be compared to table 2 in the first article.

The selection of commands also differs, although the main command menu still resides on the right side of the screen. The SCMD/PNLC command is dropped from the SYMB (symbol) mode, but SCMD/SPKG, for entering the package data into a part file, is added. The LEVL command is replaced by SWAP since PC-CARDS does not support hierarchical PCB construction. SWAP has a submenu for choosing COMP (component), GATE, or PIN swaps.

PC-CARDS also includes commands to manipulate vias. A *via* is a plated through-hole in a PCB that establishes electrical conductivity from one layer to others. PC-CARDS supports the manual entry of *ratsnest* lines (or airlines) to show the direct point-to-point connection between pins on the parts transferred from the schematic to the PCB

PHOTOGRAPH • MARC DAVID COHEN

database. The status line area carries an *R* that alternates in color to indicate whether ratsnest displays are on or off.

Finally, PC-CARDS adds the DRAW/FLSH command to support photo plotting; specifically, it is used to enter data. The flash itself is represented by a default graphic dot. Users need to understand the photo plotting process in order to gain a mastery of PCB-3. A sidebar on the subject, entitled "Photo Plotting," accompanies this article (p. 164).

TABLE 1: *PC-CARDS Command Set*

LAYER NAME	FUNCTION
PADCOM	Component-side-pad graphics data
FLCOMP	Component-side-pad photo (flash) data
PADSLD	Solder-side-pad graphics data
FLSOLD	Solder-side-pad photo (flash) data
PADINT	Internal-layer-pad graphics data
FLINT	Internal-layer-pad photo (flash) data
GNDCON	Ground-plane-strap graphics data
FLGCON	Ground-plane-strap photo (flash) data
CLEAR	Universal-clearance graphics data
FLCLER	Universal-clearance photo (flash) data
PWRCON	Power-plane-strap graphics data
FLPCON	Power-plane-strap photo (flash) data
SLDMSK	Solder-mask graphics data
FLSMSK	Solder-mask photo (flash) data
DRILL	Fabrication-drawing-drill symbol or number
FLDRIL	Drill-target photo (flash) data
PIN	Pin- or via-color-select layer
BRDOUT	Board-outline graphics layer
FLTARG	Reference targets for film alignment
SLKSCR	Silk-screen shapes or data
DEVICE	Device number graphics
ATTR	Attribute data
REFDES	Reference designators
COMP	Component-side traces
SOLDER	Solder-side traces
INT1	First internal layer traces

The major editors available in PCB-3, PC-CAPS (on the schematic end) and PC-CARDS (on the PCB layout end), have fairly similar command sets. Thus, the user can operate both editors without having to completely relearn the program.

PARTS AND PART LIBRARIES

The standard layer structure in PC-CARDS, in both the libraries and the manuals, is different from that of PC-CAPS (see table 2). In many respects the structure is parallel to hand-taped PCB layouts: some layers serve as pad masters, some as trace masters, some as silk screens, and so on.

The first 14 layers of the database are used for data that support the two output methods. For pen plotting and dot matrix printing of the pads, thermal reliefs or straps, and planar clearance information, true graphics symbols are required. The flash information for photo plotting is stored in a different manner. This results in a dualism of data to describe these entities, because the pen plotters and dot matrix printers do not have a means of interpreting PCB-3 photo plot flashes.

P-CAD offers an extensive set of parts libraries. Their use makes the creation of a part using PC-CARDS simple, even though some areas of the procedures are rigid. The P-CAD libraries use a scale of 1 DBU (database unit) to 1 one-thousandth of an inch. Although another scale may be used, this one will accommodate most of the work for through-hole design and reduce inaccuracies caused by creating libraries from scratch. However, it may not be adequate in some design sectors. (Users may generate their own libraries, but the development requirements of such a task are immense.)

The parts creation process suggested by P-CAD begins with the layout of the pins. Then the silk-screen outline is added. Following that, the device type identifier (device name) is placed and the part's intelligence assigned using the SCMD command set. Drawing the silk-screen image is easy: the same set of handy drawing commands is used in PC-CARDS as PC-CAPS.

The operation of entering pins must be given strict attention. PC-CARDS automatically assigns the pin number as pins are entered. Unlike PC-CAPS, PC-CARDS does not automatically select layers for entering the pins or other data. The user must set the layer status manually. If he makes an error in the pin entry and catches it immediately, that pin can be deleted and the process continued. Otherwise, all pins should be deleted and the pin entry process started over.

This autonumbering of pins does not allow for the irregularities present in the real world. One example is chips such as oscillators that are contained in packets the size of a 14-pin, dual-in-line package (DIP). Convention may dictate that the four physical pins of such a part be numbered 1, 7, 8, and 14, but P-CAD numbers them 1, 2, 3, and 4. The PCB-3 system sees that only four physical pins are present and is designed to consider industry naming conventions as incidental. Another problem surfaces with dense pin grid array (PGA) or connector parts that use alphanumeric numbering schemes—P-CAD does not accommodate such problems.

The system lets the user specify the pin type and logic equivalency at entry or in a batch mode later. The user is prompted for a pin name location. Many times the pin names are not shown, so P-CAD allows the user to escape this prompt (via ESC) and enter the pin name only. If pin names are displayed, the text attributes can be changed during the process.

Setting the pin type in a batch mode is accomplished using the SCMD/SPAT command. This enables the user to specify which pins are logical equivalents to the pin in the part. The ability to later swap pins depends upon these equivalency data. The parts file also defines the gates, using SCMD/SPKG. This command invokes a prompted data entry routine that asks for the number of gates, the number of pins per gates, the name of each pin in the gate, and the location of each pin in each gate. The ability to swap gates at a later time depends upon these data.

Another point in parts file creation is the assignment of a component type ID. P-CAD supports only the major classes of components, grouping the remainder into three inexplicit categories. Distinct, conventional types are assigned to DIPs (chips with *U* reference designator class letters), resistors (*R*), capacitors (*C*), inductors (*L*), and transistors (*Q*). The other three component classes

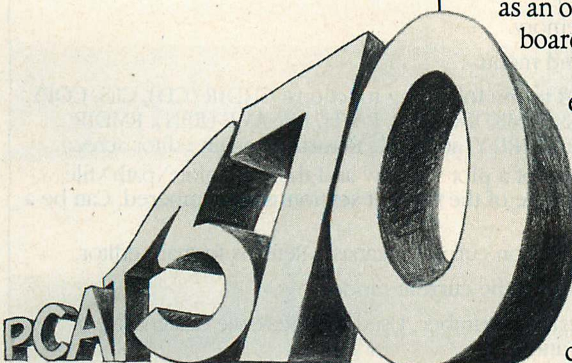

TABLE 2: *Layer Structure for PC-CARDS*

MAIN COMMAND	SUB-COMMAND	SYMBOL MODE	DETAIL MODE	DESCRIPTION
SYMB		●	○	Sets symbol mode environment.
DETL		○	●	Sets detail mode environment.
FILE		●	●	Invokes FILE subcommand menu to perform filing and memory clear operations.
	SAVE	●	●	Saves current file. Prompts \path\file name. Remembers the previous entry during session to save keystrokes for updates.
	LOAD	●	●	Loads a file into RAM. Prompts like SAVE.
	ZAP	●	●	Clears current database memory.
SYS		●	●	Invokes system subcommand menu.
	DOS	●	●	Invokes a DOS shell limited to the following functions: CHDIR (CD), CLS, COPY, DATE, DEL, DIR, ERASE, FIND, MKDIR (MD), PATH, RENAME (REN), RMDIR (RD), SET, TIME, TYPE, VER, VERIFY, and VOL. Returns to main editor screen.
	PLOT	●	●	Prompts for opposite corners of a plot window and then the plot \path\file name. The last \path\file name of the current session is remembered. Can be a help or a hindrance.
	STAT	●	●	Displays window with statistics on current database. Returns to main editor.
SCMD		●	●	Invokes subcommand menu for the current mode.
	SCAT	●	○	Prompts for component attribute number. Used for reference designator, simulation, package status, and so on.
	SPKG	●	○	Prompts to set the logical packaging and pin assignments enabling packaging of schematics. Sequential operation, must step through all prompts to use.
	SNAT	○	●	Prompts to set global net attribute, for example, PWR, GND. Has no valid use in PC-CARDS.
	GSSF	○	●	Calls or removes user-defined pad-stack graphics.
ENTR		●	●	Invokes subcommand menu for current mode selected.
	PIN	●	○	Prompts for the pin location, pin name location and pin name. Allows nonplacement of name. Stays in mode until new command is selected.
	ORG	●	○	Enters symbol origin (*0,0*) from which all other data is then made relative. Usually is on lower left pin in libraries.
	COMP	○	●	Prompts for file name of symbol to be entered, then prompts for placement. Allows scaling of symbol in x and y axis as well as rotations and mirroring. Default reference designator assigned by system, not displayed here. Pressing F4 during process allows user to assign component name. Stays in mode until new command is selected.
	WIRE	○	●	Prompts user for starting, then next points on wire. Assigns default net name automatically. User can press F3 to assign actual name during process. Wires are intelligent, checks for shorts or merges during input. WIRE layer is selected automatically. Allows style variables to be changed. Entry by pointing or direct coordinates.
	RATN	○	●	Defines a net or net segment between two points or more with a ratsnest line.
	UCOM	○	●	Uncommits a pin from a placed net. Helpful edit tool.
DRAW		●	●	Invokes subcommand menu. Stays in mode until new command is selected; subcommands also operate this way. Line style and widths can be changed when operating subcommands. Entry by pointing or direct coordinates for subcommands.
	LINE	●	●	Same as WIRE without net intelligence. User selects layer for placement.
	RECT	●	●	Prompts for opposite corners, draws rectangle.
	FREC	●	●	Fills rectangles.
	CIRC	●	●	Prompts for center and radius points, draws circle.
	ARC	●	●	Prompts for center, radius, and end point. End point snaps to arc radius on any defined radial line.
	TEXT	●	●	Prompts for location and text string. Allows attributes to define size, orientation, justification, and mirroring.
	FLSH	●	●	Prompts for location of flash number attribute and graphics. Flash number is set on the status line.
NAME		○	●	Invokes subcommand menu.
	COMP	○	●	Prompts to select component symbol and enter name (reference designator or other text).
	NET	○	●	Prompts to select net and enter name. Checks for violations and prompts for merges.

MAIN COMMAND	SUB-COMMAND	SYMBOL MODE	DETAIL MODE	DESCRIPTION
ATTR		●	●	Invokes subcommand menu.
	SCHG	●	●	Prompts to select and change attribute.
	ACOM	●	●	Attributes a component or a schematic as a whole.
	DATR	●	●	Prompts to select and delete an attribute.
EDIT		●	●	Invokes subcommand menu for the mode selected. Stays in mode until new command or subcommand is selected. Used for wire and line manipulations.
	ADDV	●	●	Adds a vertex
	DELV	●	●	Deletes a vertex
	MOVV	●	●	Moves a vertex
	MOVA	○	●	Moves whole wires only.
	DELS	●	●	Deletes a segment.
	LAYS	●	●	Changes the layer of a segment.
	MOVS	●	●	Moves a segment. Does not detach intelligence for wire segments moved.
	AVIA	○	●	Adds a via at a vertex.
	DVIA	○	●	Deletes a via.
	MVIA	○	●	Moves a via.
MOVE		●	●	Invokes subcommand menu, but can be used to move single objects except wires. MASK command observed also. Stays in mode until new command or subcommand is selected.
	WIN	●	●	Prompts to define a rectangular window of objects for moving. Rubberbands wires not entirely in the window. Moves net names on moved wire segments.
	IDEN	●	●	Identifies objects, except wires, and moves them.
ROT		●	●	Invokes subcommand menu for WIN and IDEN actions like MOVE. Allows single object rotation without subcommand selects. Rotates at 90-degree increments from user-defined origin.
COPY		●	●	Invokes subcommand menu for WIN and IDEN actions like MOVE. Allows single object copy, including wires. Wire copy includes net name text location but deletes text and net associativity. Single-point pick-up includes all wire segments on the wire that are merged to it. COPY/WIN does not observe MASK settings and requires all wire or line segments to be in window during copy.
DEL		●	●	Same as COPY, except performs deletes.
	UNDO	●	●	Undoes last delete action. Does not apply to EDIT/DELS actions.
CLYR		●	●	Same as COPY except performs change layer actions to selected layer.
SWAP		○	●	Invokes SWAP submenu.
	PIN	○	●	Swaps logically equivalent pins.
	GATE	○	●	Swaps logically equivalent gates.
	COMP	○	●	Swaps component placements. The ratsnest of each component is displayed before and after swap.
ZIN		●	●	Software zoom in, multiple levels, accepts multiple zoom steps before redraw according to timed entry of execute commands. User defines center of view by pointing or coordinate entry. Stays in mode until new command is selected.
ZOUT		●	●	Reverse of ZIN.
VWIN		●	●	User defines rectangular view to be redrawn on display.
REDR		●	●	Redraws the display. Requires a higher-level command change to display new information in some cases.
PAN		●	●	Pans display window to center on user-defined location. Stays in mode until new command or escape is entered.
LPAN		●	●	Produces screen for selecting long range pan in the database.
STO		●	●	Stores nine views and a map view of portions or all of the database.
RCL		●	●	Recalls stored views and map.
VLYR		●	●	Views and alters layer structure.
MASK		○	●	Masks components and/or wires from some command actions.

● = *Yes* ○ = *No*

The information required for the photo-plotting process is stored on separate layers to the graphics data that would be required for traditional pen plotting of PCB masters. The PC-CARDS structure is more parallel to hand-taped PCB layout.

offered by P-CAD deliver essentially meaningless letters for parts classified as other discretes, connectors, or miscellaneous. Because these letters are used to annotate and back-annotate schematics, the schematics will require manual correction for adherence to the ANSI Y32.2 industry-wide standard.

The final item to consider with regard to parts is individual file size. The PCB-3 system takes up a larger file size than many of its competitors.

PADSTACKS

Correctly sized pads are a key to creating successful PCBs. The holes needed to mount the parts on a particular PCB, and their associated pads, will be a variety of sizes. The PC-CARDS scheme uses the pin type number as a reference for importing data to create the pads in the PCB database. These imported data are called a *padstack*.

A padstack is a graphics and data overlay file, similar to a parts file of a single pin part, without the pin. It contains the graphics and flash data located on each of the necessary pad layers. The data are located by centering them on the same coordinates in each layer as if a pin were there.

The principal means of letting the system know which padstack data are to be overlaid (and where) is the pin type number. In PC-CAPS, the pin type number specifies the electrical activity of a pin—input, output, or both. PC-CARDS uses the pin type with a cross-reference file to determine which padstack data will be assigned to the pin at every occurrence of the pin type on a part (and later in the PCB database). P-CAD offers 25 types (type 0 is reserved for vias).

Situations will arise outside the limits of the padstack scheme. Thus, the user needs to be able to send the pad data to the design through the parts file in the library. This is necessary also to get around the numerical limitations of the 24-position Gerber system. The user can embed data to be pen-plotted for pad construction or flashed by a photo plotter in the parts file. These data may be additional to, or replacement for, the data to be imported from the padstacks later. Nevertheless, the assigning of padstacks to a pin type allows for flexibility in the use of the libraries. It averts, for example, the need to produce a library of parts files for each customer who requires a different pad style for pin 1 on DIPs. These specifications can be met instead with a single parts library and different padstacks.

The relationship of padstacks to pin types is stored in a cross-reference file with the extension .SSF (special symbol file). The SCMD/GSSF command imports the padstack data, which it links or unlinks from the database. This feature enables the user to create several sets of padstacks that are referenced by various .SSF files for various purposes, such as different customers or design rule checking. The .SSF allows for different padstacks for the same pin type, depending on the connectivity of the pin to a net. For example, by creating different graphics for a pin that is connected and one that is not, unused pins can be recognized easily during the PCB creation cycle.

LAYOUT IN PC-CARDS

PCB-3 can work in a variety of ways to generate PCBs. PC-CARDS can be used by itself to produce PCBs, with or without data imported from PC-PACK. Alternatively, PC-PLACE and PC-ROUTE can be used in conjunction with PC-CARDS. Layout from within PC-CARDS is performed in DETL (detail) mode.

Users should note that PC-CARDS does not always display a complete image. The program draws portions of the image that are critical in most situations. The fact that it does not display them during the operation of PC-CARDS is sorely missed in the construction of wide traces or drawn planes. Worse, P-CAD does not document this limitation in the PCB-3 manuals.

Placement begins with the creation of a board outline. If the database has been packaged using PC-PACK, the user moves the components (via MOVE) into the PCB outline area. Placement of packaged parts is partially aided by the display of ratsnest lines of each connected pin. By studying the ratsnest pattern, the experienced designer can move parts around to shorten trace runs, alleviate congested areas, and create an easily routed design. Sometimes the displayed ordering of the ratsnest lines will produce a screen that is difficult to read. In the design of a PCB with power and ground planes, for example, the user may wish a means were available selectively to turn off nets.

PC-CARDS includes the PC-CAPS error-checking facilities, which check for unwanted net merges and connections to assigned pins. But seeing where the route is headed is also helpful. PC-CARDS displays this in the initial route of the points during the hook up of the net. If, however, the trace is edited—for example, by the deletion of a segment and addition of other segments later—PCB-3 exhibits another idiosyncrasy. When the user attempts to

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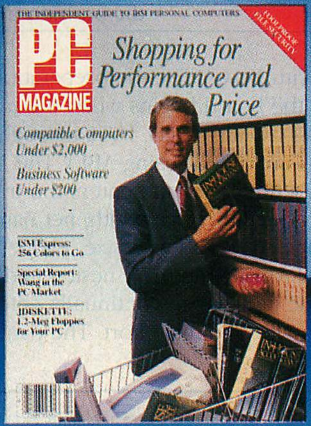

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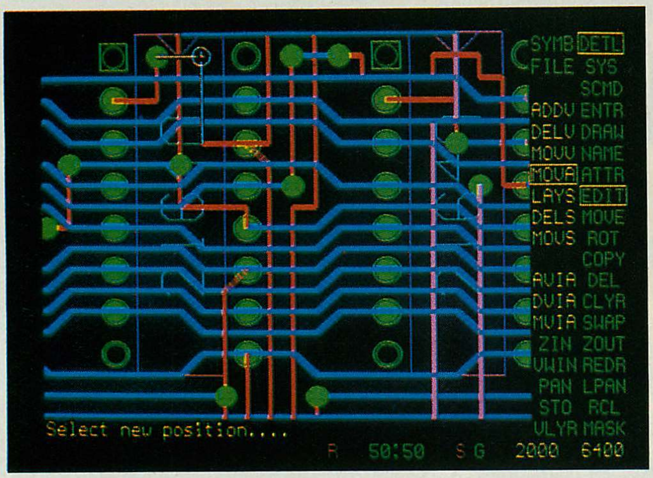
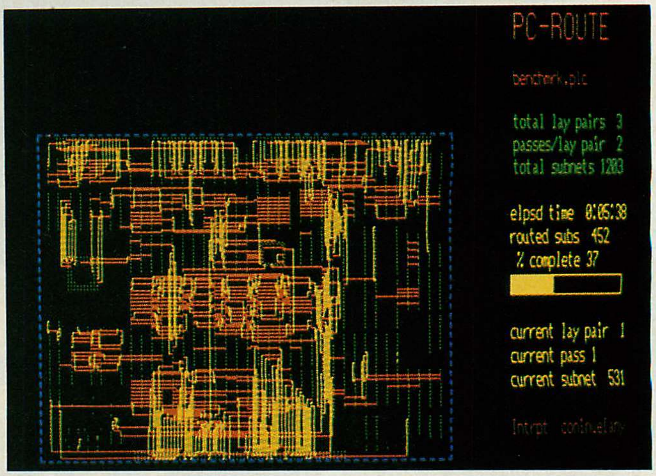
PHOTO 1: *PC-CARDS Screen*



PC-CARDS includes commands to edit vias, which are not used in schematic layout. MOVA, for example, moves the vias along with their attached wire segments.

PHOTO 2: *PC-ROUTE Screen*



PC-ROUTE displays the status and the route; the status only; or the status, the route, and the wavefront that represents the position in which the router is trying to place the next net.

recomplete the route, the points on the net are highlighted, but they turn off after the second vertex is entered. Thus, a supposedly helpful feature becomes nothing more than a frustration.

When ratsnests are used, one is deleted from the full display of active ratsnests each time a net is completed. Thus, the user has a visual confirmation of the remaining unrouted nets.

With PC-CARDS, the preparation to route the board begins when the trace layers—COMP, SOLD, INT1 through INT*n*—are abled (using ABL). The ENTR/WIRE command enters the traces at the specified trace width, net name and line style, and grid size. ENTR/WIRE and DRAW/LINE remain nested and thus provide a means to continually enter traces with minimal effort. The pan and zoom commands are not automatic and must be selected from the menu. This limitation impairs smooth routing performance because it adds to routing time. An option to pan continually would be a good addition.

The user may have routing design rules that require all corners to be at 45 degrees, or 90 degrees, or to allow any angle. PCB-3 accommodates these designations, but the choice must be toggled from the status line.

P-CAD provides tools to erase traces or trace segments, to move or copy them, change their layer, or alter their configuration. In PCB design, however, the presence of vias adds another dimension. The EDIT subcommands provide for adding, moving, and deleting vias. The MOVA and LAYS subcommands can interact with vias; MOVA, for example, moves a via along with its attached wire segments (see photo 1).

LAYS changes the selected line segment to the active layer. If this results in both ends of the segment being connected to wire segments on other layers, vias are inserted automatically at the joining vertices. However, in some instances when a pin is at such an intersection, the via also is placed on the pin. The user then has to correct all instances of vias on pins, using the DVIA subcommand, before extracting film and pen-plot data from the database. An internal via-on-pin delete routine would alleviate this problem.

The system's handling of power and ground planes is not automated; even so, the end result works. The actual connection is made on the film plot using flashes for thermal reliefs and straps. The connectivity informa-

tion, therefore, is not entered into the PC-CARDS database because flashes are not recognized as wires. One way to ensure that the information does get entered and is shown as completed is to connect the points with wire on a database layer not used for the final film. Users should note, however, that this method does build in a potential for error, such as wires that are entered without an associated flash.

Another bug in PC-CARDS sometimes surfaces during frequent activity in one submenu. The user makes the first selection, then he may choose a second, and continue down the menu. When a second submenu item is selected, the first one retains its box, in a different color. This box can expand to include the entire subcommand menu; the user can lose track of which command is truly operating.

Although not a bug, an annoying quirk occurs when nets are entered using ENTR/RATN. As a net is entered from pin to pin, it overwrites itself and disappears. This same problem occurs during routing with ENTR/WIRE. Both of these situations can be reversed by selecting redraw, but that is an inefficient process at best.

Other than these difficulties, PCB routing with PC-CARDS is clean and easy. PC-CARDS accommodates a maximum of 500 components, limited to 300 unique types, and a maximum 6,000 pins, with 2,100 maximum in the buffer.

The pin limit provides that, in theory, a PCB of nearly 132 EICs (equivalent integrated circuits, which are based on 16-pin DIP ICs) causes paging to occur until the 6,000-pin or another limit is reached. The limits for other elements are 6,500 picture groups (2,100 cause paging), 47,000 picture elements (15,000 cause paging), and 1,000 nets in a database. Actually, databases with more than about 60 EICs become increasingly slower at posting information and redrawing as they near design completion. Then, as they approach 80 EICs, they go into paging, unless the balance of the other database elements has forced paging already.

One of the nicer end-to-end touches in PCB-3 is the operation of NAME/COMP on a database that has been packaged by PC-PACK in PC-CARDS. This command enables the user to make visible and place in the PCB layout the reference designator of a part as it was assigned in the schematic or during the packaging process. However, the package offers no equally easy method of accomplishing the reverse—that is, of transferring the reference designator renumbering that is commonly performed in PCB layout through back annotation to the schematic.

PC-DRC/NLC. Another key element in successful PCB-3 design is the PC-DRC/NLC (design rule checker/net list checker) utility, referred to here simply as PC-DRC. This program checks for design rule spacing and size violations and the continuity of wired nets in a design against the packaged net list. PC-DRC requires an input database that has acceptable padstacks attached.

PC-DRC enables the user to specify the spacings and layer groups to be checked. Spacings are stored in a file called a *rule set*; groups of layers to be checked together are called a *pass set*. These sets follow certain conventions in connection with each other: Each pass set has a rule set attached to it. The user may create a new pass set and attach an existing rule set to it, but when a rule set must be changed, it must be modified for each occurrence in the pass sets. Rule sets can be created, saved, edited, and deleted.

Each set has nine specifications that are checked: round pad size, nonround pad size, via size, trace width, and the spacing from pad to pad, pad to trace, trace to trace, pad to board edge, and trace to board edge. The pad size and trace width parameters establish the minimums for the check—any size or width under these is reported. Width violations are reported until a maximum of 50 is reached. The spacing parameters run from edge to edge of the objects tested. PC-DRC tests all objects, including drawn lines and text, for trace-spacing violations; however, it does not provide a much needed via-to-via check parameter.

The continuity of the wires of each logical net can be verified using the continuity checking option. This test is valid for layouts that were not functionally modified during the PCB creation, thus, the net list obtained from PC-PACK and the swap data together represent the true circuit.

The results of a PC-DRC check are generated in both graphic and report form. The graphic indicators are added to the database on two layers. The first layer, $DRC, reports the design rule violations by highlighting the object errors. The second layer, $CONT, uses airlines to highlight unwired or disjoint nets. Because $DRC displays all errors, regardless of the layer in which they occur, the user may find the information overwhelming in the case of dense designs that have many errors. The DRC report alleviates this situation.

PHOTO PLOTTING

The traditional method of producing printed circuit board (PCB) layouts by hand-taping onto mylar, then photographically producing an image that is used as a mask for board, is now superceded in two ways.

With the introduction of computer-aided design (CAD), hand-taping has replaced pen plotting. The taped image is produced on mylar with a pen plotter; film for making PCBs is made by photographing pen plots of the PCB design. This method does not work well for many designs, however, and it is not always cost-effective. It is dependent upon plotter accuracy, board density, routing grid density, and board manufacturing tolerances.

An alternative method is to use a photo plotter. The data from a CAD package is output in a form that can be used to drive a photo plotter. The standard Gerber photo plotter uses a light source directed through a transparent image in a piece of developed precision film depicting a shape called an *aperture*: an aperture is a hole the shape of the desired image to be plotted. Depending upon the film media used for the PCB plot, either a positive or a negative image will be plotted. Apertures generally are round or square, but special apertures for making asymmetric pad shapes, thermal relief ties for planes, drill target symbols, and so on, also can be used. Gerber photo-mechanical plotter systems support 24 apertures per wheel.

The aperture, mounted on a movable wheel, is positioned between the light source and the film. Each command to the photo plotter is either a *flash* or a *draw* of a particular aperture. For a flash, the machine moves the table holding the film to the position required, then the light is turned on and off. For a draw, the aperture is selected and the light is turned on at the initial position for the line, then the table is moved in the directions needed to produce the final image. Because the light is on continuously during drawing, the apertures for drawing have filters to impede the transfer of light through the aperture. This serves to control light bleed (or overexposure) of the film, which otherwise would distort the image.

Other photo plotting systems use similar schemes to produce the same results. Some do not "flash" a flash image, they draw it instead. The Gerber method of coding this information as flashes and draws is a de facto standard for transferring data even to non-Gerber systems, including rasterizing laser photo plotters.

A Gerber photo-mechanical system operator typically charges a designer for plotting time and materials. The time expense for plotting using this method is proportionate to the number of images plotted and the optimization of the plotting path to save bed movement time between flashes and draws. The photo-mechanical method is now getting competition from laser photo plotting technology, but from a cost standpoint only—the production quality is on an even par.

Laser photo plotters usually accept Gerber-coded files. These files are cross-referenced to aperture image files. The data are processed into a file that represents a rasterized image of the entire plot. This processing is fast and efficient. The image is plotted raster line by raster line on the film. Because a raster image plots faster for the majority of PCB film, and because it plots in a fixed time, the charges are fixed for each film size. (This usually works in favor of the designer.) An added benefit is that turnaround time from sending data out and receiving film back is shortened.

The cost of photo plotting is directly related to the efficiency of the CAD program that produces the code to drive the photo plotter. P-CAD's PC-PHOTO produces accurate, but not optimized, code. Although the coordinates to complete a draw are present, they are preempted by a MOVE command that *precedes* them, rather than trails them. This is unacceptable for such a high-priced program.

—Richard Angell

PC-DRC actually produces two reports, one for the continuity check and one for the rule check. Each report yields information to determine the rule set, DRC performance, database statistics, and type of error. The DRC report includes the type of error, the offending value, the entities involved (such as PAD, VIA, or TRACE), and their locations. DRC detects an error when text or an identification symbol is placed near the PCB edge. This may be acceptable for the design, but no means are available to exclude such items from space-to-edge checks.

PC-DRC does have reporting limits—the trace-width error limit, for example. Another limit is that for any one pin type, only the first pad or via size error is reported. If too many errors are discovered, the check aborts and the first error list is produced.

PC-PHOTO. Menu-driven PC-PHOTO takes an object from database plots to finished film. It accepts the plot file as input and processes it into a format for the end peripheral. This output is saved to disk files for the Gerber model 32, 33, and 41 photo plotters. PC-PHOTO can drive the GTCO FP1-1622 and Patek Philippe Flashscan photo plotters directly. The opening menu has the standard three choices: configuration, operation, or exit, with an additional selection to configure an aperture table. The configuration files are generated only if the user changes default values.

The operation menu allows specification of the input file and changes to the configuration for a particular plot. It lets the user see the maximum magnification that can be plotted (scale factor), select a suitable size in the range, and specify plot orientation: either normal or rotated 90 degrees.

PC-PHOTO generates an error file if it finds illegal information in the input. Such information would include lines drawn smaller than the smallest available aperture.

This completes the list of program modules necessary to create a PCB using PCB-3. For analog design, these programs may be all that is needed (they are available as PCB-2 for about one-third less than PCB-3). The other two PCB-3 modules, PC-PLACE and PC-ROUTE, are used mainly for digital circuits, but can be used for mixed digital/analog and analog designs.

PC-PLACE

Placement and placement analysis tools are provided by PC-PLACE in an environment that is similar to PC-CARDS, and with many of the same commands. PC-PLACE operates in the DETL mode environment. The first new item the user is likely to notice in PC-PLACE appears on the second screen—the added selection, Edit Part Footprints.

PC-PLACE requires an attribute, called a *footprint*, for each part in a database. This footprint is the class name of the part—for example, DIP 14

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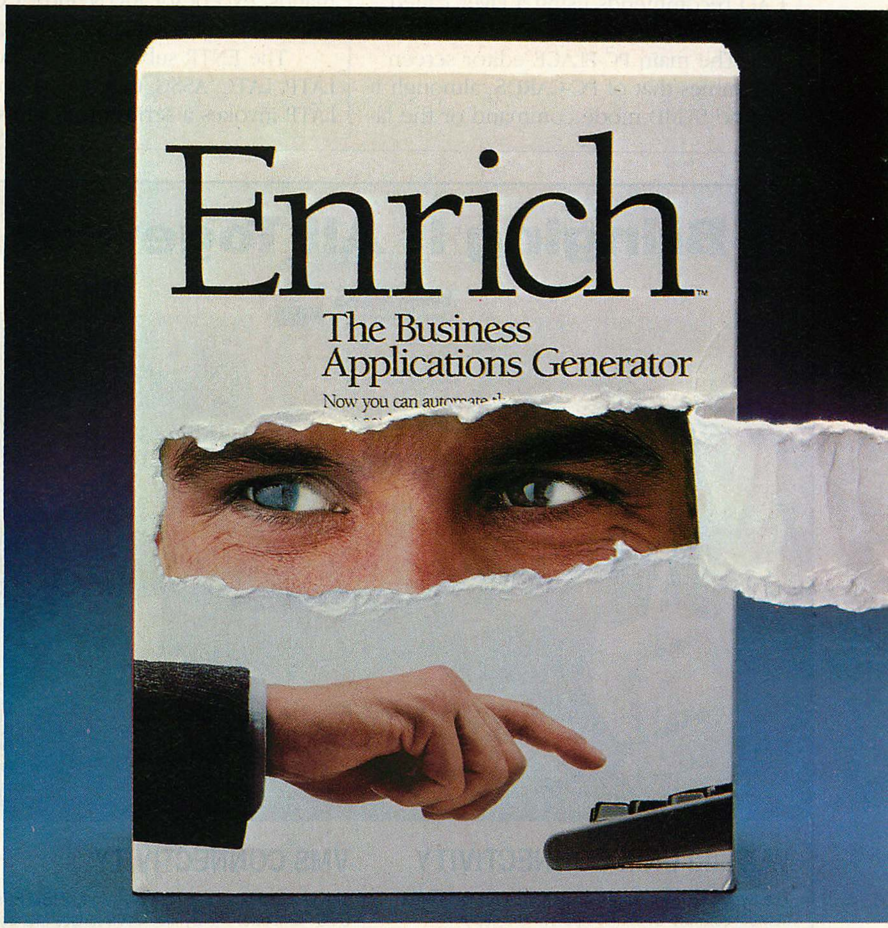

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for 14-pin DIP parts. The attribute then is assigned to parts with the same physical footprint. Selecting Edit Part Footprint invokes a menu and prompt editor to view, add, modify, or list parts footprints in the parts files in a library. To view the footprints, the attribute FP = <footprint class> must instead be assigned to each part in PC-CARDS. P-CAD recommends using a layer called FP for this purpose.

The main PC-PLACE editor screen resembles that of PC-CARDS, although it has no SYMB mode command or the familiar ATTR, COPY, CLYR, or MASK. DRAW/FREC also is gone, and SCMD has only the GSSF subcommand. This program adds the commands PLCE, HIST, ALGN, FIX, and QRY. These activate, respectively, autoplacement, aids and analysis tools, component alignment tools, and data inquiry commands. ENTR has a whole new set of commands, except for RATN and UCOM. Many new subcommands are added.

The ENTR subcommands include LATP, LATC, ASSC, CLR, PARM, and CUT. LATP invokes a series of prompts to define part placement lattices. A *lattice* is a regular set of points, at defined incremental (*x* and *y*) spacings, that are in a defined rectangular area. PCB-3 displays a lattice as intersecting orthogonal lines.

Multiple parts placement lattices can be defined; each lattice adds one more layer to the database. If the user does not establish the layers, then PC-PLACE creates and ables (via ABL) a layer it calls LAT1. When the user needs multiple lattices—LATMAJ for major parts (such as DIPS and connectors) and LATMIN for discretes and other minor components, for example—they must be created. The user ables (via ABL) the appropriate layer and uses ENTR/LATP to establish its lattice. The lattice must be within the PCB borders. Later, during the PLCE operation, the part origins (usually pin 1) will be placed on a lattice point if one is available and if it meets other criteria. A lattice that has, for example, too many points, causes PLCE to abort because of memory allocation constraints.

Other criteria in the ENTR command set establish which footprint class of parts is to be placed on which lattice (LATC). They define where a discrete can be placed relative to a major part (ASSC) using the selections ABOVE, BELOW, LEFT, or RIGHT and a clearance spacing. The CLR command permits the specification of *x* and *y* ordinal clearances for major parts.

ENTR/PARM allows parts to be sorted for placement based on height or width and a percentage index of the predominance of part footprints on the lattices in the database. This predominance, called a *constraint ratio* by P-CAD, is the quantity ratio of a footprint class to the available lattice points for their placement. For example, with 50 components in the class and 100 lattice points, the ratio 50:100 would be 50 percent. If the user establishes the *constraint index* (a cutoff constraint ratio value) for the whole database at 60 percent, these parts would be placed after those with a ratio of 60 percent or above. The higher the percentage ratio for a particular part, the more constraints on its placement. The ratios require manual derivation, which may discourage fine-tuning of this parameter.

With ENTR/CUT, the user can establish *cutlines* in the database; *cutlines* divide the PCB horizontally or vertically into partitions. PC-PLACE tries to place circuit-related components within the partitions and minimize the number of nets that cross the lines. The cutlines cannot be seen, but they are listed on one of the PC-PLACE reports. The sys-

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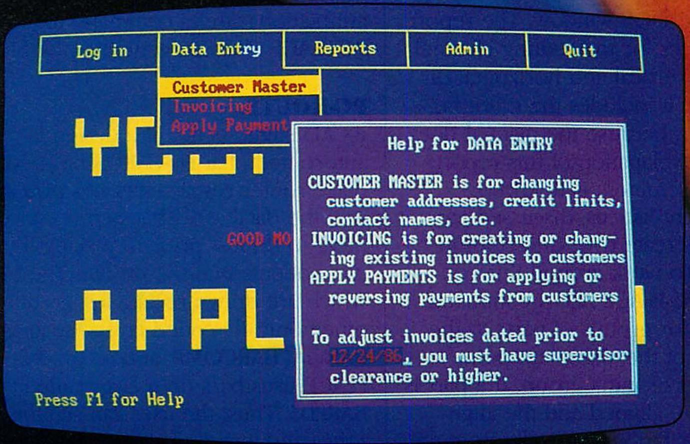

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tem can and will allocate and specify cutlines itself, and P-CAD recommends letting the system do the cutting. Cutlines are a feeble means of circuit segregation. Although useful in some designs, they are not likely to ease analog design placement needs.

One quite useful command is FIX, which allows the specification of parts that are not to be placed by the program, but are to remain in a user-designated location. The fixed parts are highlighted when the command is selected. A fixed part can be unfixed by selecting FIX again. This command is a necessity for connectors and critical components.

These manual placement tools are somewhat limited. They do not provide for the specification of discrete-to-discrete clearances, nor is there a way to identify special circuit groups. If such a means were available, it would logically start with schematic annotations in PC-CAPS. This missing ability can make it difficult for the system to place analog designs of any complexity.

PC-PLACE provides histogram and force vector methods of placement analysis. The force vector of a part (a vector summation for the part's nets) is another factor that can affect placement. Force vectors are placed in a layer called $FORC. They toggle on and off according to user input to a status line prompt. The visual image is a line vector from each part's center, terminated by a circle indicating the part's best position for short routes, based on the placement of other parts in the design. If the part is moved to such a location, this changes all parts vectors. Also, because the power and ground nets cannot be ignored or turned off, their force is added into the vector summation. This detracts from finding the true position of a component.

The histogram placement in PC-PLACE is loaded by selecting the HIST command from the main menu; it is configured using the CNFG subcommand. This sets up the basic configuration, including number of layers, routing grid, and channel resources for displaying the histogram and force vectors. The histogram is a graphic bar chart displayed on one vertical side and one horizontal side of the editor window. The bars are oriented in the direction of the channels that they represent.

The histogram display presents calculated usage for horizontal and vertical routing channels in a defined routing grid area. The display uses either narrow or wide bars to communicate the information: the narrow bars provide a clearer picture. The length and color of the bar also is significant. In the default color scheme, a green bar represents 0- to 35-percent channel usage; a yellow bar, 35- to 50-percent, and a red bar, over 50 percent. The length of the bar indicates the place in each range in which the channel usage currently falls. The histogram size can be set for 8- to 20-percent of the viewing area. At the common vertex of the histogram axis, a box with a numeric value (called the merit factor) is displayed. Each time the user makes a change, the histograms and merit factors are recalculated to show the effects. The merit factor is a number that is relative to the impact of the change: it must be compared to the last number to be meaningful.

Calculating and displaying each new histogram and merit factor takes time. The larger the design in terms of parts and nets, the more time is required. Such delays interrupt the process by distracting the user, and can leave an adverse impression of this powerful analysis. If the force vectors are being displayed as well, they also will take time to recalculate and display. The user can speed up this process somewhat by displaying force vectors from major components only.

FIX, a useful command, allows the specification of parts to a user-designated location, rather than their being placed by PC-PLACE.

The only other subcommand to HIST is STAT, which generates a report that the user can view or print through the PC-PLACE DOS window. The report contains values for the routing channel demands in vertical and horizontal directions, and it includes the merit factor. However, because the manual does provide an explanation of this report, its relative usefulness is unknown.

Placement lattices, discussed earlier, tend to create rows and column placement. To work around this constraint, the PC-PLACE ALGN command aligns a part or groups of parts to the farthest axis of the alignment point from the part or parts group. If a part is selected to be aligned and the alignment point is farther vertically from the part, the part will be moved and aligned to the y axis of the specified point. Thus, aligning a part or group of parts to a particular point can take two steps. ALGN has an UNDO subcommand that reverses the procedure.

The QRY command has a submenu of COMP (component), PIN (pin), or NET (net). Each command displays information about the particular items. The handiest QRY may be QRY/NET, although using QRY/PIN to discover pin type and logical equivalency assigned to a part will also be quite helpful (when it works in a future version).

The remainder of the commands are similar to those in PC-CARDS. Some add an UNDO function, and the MOVE command has a COMP subcommand.

The final task required of PC-PLACE is for it to place the parts optimally for ease of routing and circuit segregation. The PLCE command attempts to do this by invoking the automatic placement routine. PC-PLACE can be successful with smaller digital designs; however, as the design begins to include some analog or becomes all analog or otherwise very dense, autoplacement may become a less appealing elective.

A PC-PLACE report provides information about the placement effort. It includes statistical information about the PCB relative to chip; discrete and connector quantities; total component count; estimated total trace length to connect the design, EIC quantity, and EIC density. The report lists cutline coordinates, warning messages, and lists of placed and unplaced components. The placed components list includes the reference designator, parts name, and an x,y coordinate for the placement. The coordinate list bears little resemblance to the real placement of the part. It is apparently derived from the origin of the part, which may or may not be pin 1. Time performance statistics are included. Other reports include one for errors, one for swaps (for back annotation), and a command log file. PC-PLACE also can generate plot files.

PC-ROUTE

P-CAD suggests that if a design is to be autorouted, that PC-CARDS be used to place router restricted zones or *bars* into the database. This step is convenient to do just prior to placing the components into the design. The bars, which are drawn rectangles, go onto mnemonically coded layers, such as BARVIA, BARCOMP, and so on. PC-PLACE uses bars on a layer called BARPLC. Thus, the user can see the zones and avoid placing parts in them.

The bar information can be added to the database before PC-PACK is used.

Such a database is then used as the input layer structure to PC-PACK, so the information is in the database already. This makes sense for CAD operations using standard board configurations such as the Eurocard, Multi-bus, Std bus, and so forth.

PC-ROUTE is a batch mode autorouter, although it can be used (albeit awkwardly, and with induced aborts) as an interactive router. It offers on-line help during parameter set-up—a crucial ingredient, for although its operation is not complex, some extra attention is needed to prevent input errors.

The input database must be clean. If any routes have been made previously, they should be entered to complete their nets. Such routes are called *preroutes*. It is better for PC-ROUTE if all of the preroutes are on-grid, even though it can route off-grid. Any bar zones must be identified in order to prevent traces or vias from occurring within them. In addition, the border and parts placement requirements must be observed. PC-ROUTE requires that all nets in a database be named. If the user adds nets to the database following PC-PACK, they must be named; otherwise, PC-ROUTE will abort.

PC-ROUTE defines a routable area that is 0.1 inch inside the board outline on the BRDOUT layer. This would be fine except that it uses this area to define its routing coordinate grid system. If the PCB outline does not lend itself to a standard routing grid, such as the Eurocard outline, then a surrogate outline must be created. The actual board outline has to be placed on a different layer in the database. Although users will want the ability to set the border clearance zone to values other than the internal 0.1 inch, this is not possible. The PC-ROUTE reliance on board edges to define the routing grid requires more explanation in the documentation.

The PC-ROUTE main menu is a tree with numerous options; fortunately the choices follow logical paths. Rules and strategy are grouped together under the Edit routing strategy menu choice; the other choices are Route, Exit PC-ROUTE, and Edit router file maintenance. The last selection, which is activated by pressing the End key, permits the deletion of rule sets and files specific to a previously routed version of any of the input databases. The main menu screen also requests the entry of the database to be routed.

The routing strategy selection lets the user progress to more choices relative to a selected routing strategy file: Edit routing parameters, Edit wiring rules, Edit pad clearance rules, Help, or Escape to the previous screen.

The Edit routing parameters screen has a coarse set of rules and strategy parameters. Rules are design constraints for trace location, trace width, trace clearances, via placement, and clearances. Strategy involves several parameters: the type of routes, layers to be routed, direction of routes on a layer, area to be routed, and number of times to try routing a layer pair. Each parameter is assigned a factor that is used by the router to minimize expenses and maximize the chances for completion. The screen has provisions for specifying the main routing grid (*x* and *y* DBUs), the number of routing layers (an even number between 2 and 50), the route speed (fast or slow routing algorithms), route type (daisy-chain, Steiner, or minispan), the route order (short then long, or long then short—as explained below), and the displayed data (status only, status plus route, or status plus route plus wavefront). This menu also lets the user choose to view a detailed parameter screen.

PC-ROUTE is arbitrary in its selection of the layers that comprise a layer pair. It randomly assigns the predominant routing direction on each layer. The design can be rotated prior to

route to ensure the desired direction of routes on the final design. The layer pairs chosen are COMP and SOLD, INT1 and INT2, INT3 and INT4, and so on. In each pair the route direction is horizontal for the first layer and vertical for the second. Although this is acceptable in a PC router of this level of maturity, users sometime will want to specify the layer pairs themselves.

The terms *short* and *long* refer to the physical span length of a subnet (a part of a net). The subnet, usually the section between two pins, is a basic algorithmic unit that is used in generating wiring routes. Subnets are sorted from the shortest physical distance to the longest, or vice versa, according to the order that is selected. The router attempts to route each subnet in that order. The short-to-long selection typically connects more subnets, but may leave some very difficult, long subnets to route in PC-CARDS. In long-to-short routing, PC-ROUTE may not complete as many, but the short subnets left incomplete may be easier to connect. The user makes such a choice based on the particular design. The route speed parameter controls the time a router takes to search before either giving up on a subnet route or accepting an apparent solution. The trick is to determine if the quality of a board will suffer from the use of a fast route.

The *wavefront*, a display choice, describes an image of the router's search and decision pattern as it operates. The actual display always shows the status of the route and the current subnet vector. If the display is increased to show completed routes, the router slows down; if it also is requested to display the wavefront (see photo 2), it slows down even more.

The detailed routing parameters screen has seven sections: Routing grid definition, Via sites, Via lattice definition, Route search area size, Passes per layer pair, Costing, and Stub length. Selecting Routing grid definition allows the user to define the major routing grid and three acceptable offsets from that grid. This is to accommodate two or three traces between chip pads on grids that are not uniform. Any of these parameters can have different x and y specifications for nonuniform routing grids that predominate in a given axial direction. The concept is good, but three offsets is limiting.

Choosing Via sites permits vias to be placed on any grid point or only on a defined lattice (which is similar to a PC-PLACE lattice). This lattice must be incremented in subsets of the main routing grid, a limitation for dense routing designs. If the routing grid is 20 by 20 DBUs, a via grid of less than that is unacceptable. The limitations of three offsets diminishes the flexibility for positioning the via lattice.

The Route search area parameter designates the number of grid points outside of a rectangular area (or a straight, orthogonal line that is formed by two pins to be connected at the extreme corners) that the search can be conducted for a suitable pattern. This parameter could be increased as the router is used in successive trials to complete more routes on a partially completed design. P-CAD defaults this value to two grids—too many for the first pass. The router expands this area by two times the value for a second pass, four times the value for a third pass, and so on. Users might want to use zero expansion on the first routing pass, then change to one or two grid expansions and go for multiple passes.

The Pass per layer pair section defines the number of times the autorouter will continue to cycle through unrouted subnets in its attempt to route them on a given layer pair. The default is set to two; but the number the user sets will depend on the design itself and the user's experience with the tool.

The Costing section is another important control. Here the user establishes factors that guides the router's decision process. PC-ROUTE has three cost variables—for right-way routes, wrong-way routes, and vias. Right way is the arbitrary routing direction for a given layer, either horizontal or vertical. Users may like the concept, but they will not like the process required to change the parameters in the middle of a route: the route must be aborted, changed, and restarted, or data must be reextracted from a completed route with a new strategy selected. This tends to require a deeper knowledge of the software than the manual provides.

Another control is the Stub length section. With this control, the user specifies the maximum length of a trace that will connect to a via or vertex when it extends from a pad with two connecting traces. The Edit wiring rules selection from the Edit routing strategy screen is also a two-tiered situation. The first tier is the wiring rules; the second is their application to discrete nets. PC-ROUTE lets the user create as many as 10 named rules that specify the trace width in DBU and clearances in grid units. If a rule that has a zero width trace and zero clearance is created and applied to a net, the net is not routed by the autorouter. The wiring parameter of a net is specified by net name and the corresponding rule name. A maximum of 10 nets may be specified. If the net is not listed, then it is routed with the rule that appears first on the rules screen (as a default).

The other area of rule specification is Edit pad clearances (from the Routing strategy menu). This is where pin clearances are defined for the pin types, 0 to 24. The user specifies, in graphic form, where the autorouter can place traces and vias in relation to a pin of a given pin type and, by extension, its final pad. These blocking rules are depicted as two 11-by-11 matrices of zeros denoting available grid points around a plus sign, in each matrix center, designating the pin location. One matrix is for trace blocking, the other for via blocking. The user changes the zeros to ones to block the grid point from use.

The pin blocking rules menu has another subset that allows the rules to be specified on the basis of pin type and database layer. The layers correspond to the layer pairs selected in the strategy. This provides the ability to restrict trace and via placements—for example, trace placement on the solder side—by blocking an extra channel on this layer. This alleviates any solder bridging at manufacture and assembly. These items, once set, are saved in a routing strategy file.

The next action is to route the PCB. Choosing Route invokes a menu to begin the router. This menu lets the user specify whether to extract the data from the input database; if the route is new, or a restart, or to be done at all; whether to save the results; and under what name they should be saved.

Upon first entry to the router, the user is generally not concerned with the choices of this screen. If this is to be a restart or other action, then the user has to toggle the selections. The manual, however, does not explain the impact of the Extract data, Route, or Create routed database choices. One Route choice, Restart, is mentioned, but only in the context of an aborted route later in the manual.

Any route that requires the extraction of data takes a substantial amount of time to execute. During this operation, PC-ROUTE passes messages to the user explaining what is happening. If no errors have occurred, it records this information to a report file and continues. Otherwise it aborts and posts the errors to the file. PC-ROUTE must be exited for the user to view the file and determine the corrective action.

A successful extraction then leads to the successive messages allocating model, building model, building maps, ordering routes, and the chosen display screen. Again, the process continues only if fatal errors are not encountered. If an error is encountered, the chances are good that the user will be prepared to handle it. The P-CAD documentation includes some 65 pages of error messages, covering 136 categories, with 86 fatal and 24 system errors that say simply, "Call P-CAD."

Once PC-ROUTE progresses to routing, the probability of an abort due to error is substantially reduced. The route status screen provides good information, informing the user of the total layer pairs, the passes for each layer pair, and the total subnets to be routed. It provides the elapsed time, the number of subnets that have been routed, and the percentage of routed subnets. The display lists the current layer pair, pass, and subnet route being attempted. The graphic display of the route, with its wavefront option adds a proportionate amount of time to the router performance. After the router has attempted to route the unrouted subnets, it seeks to minimize vias, a marginal effort, but it does help—this is not a "rip-up-and-retry" router.

When the route is complete or is aborted by the user, PC-ROUTE extracts the data from the route and creates the output database. This creation also adds a layer (called $CONT) or updates $CONT if it has already been created. This layer contains the ratsnests of any nets that failed to connect. Then the main menu is called.

PC-ROUTE cannot be confined to route the nets in a certain area, as some autorouters permit. The BARALL layer and net rules could force some such control, but this is not the best way to accomplish the job. For testing, several PCBs in the 60- to 75-chip range were routed using PC-ROUTE. Each PCB was tried multiple times with various strategies. The router easily completed more than 85 percent of the routes on one track designs. It completed more than 97 percent on a two-track version, having been stopped only by a lack of sufficient available memory from possibly achieving a 100-percent route.

The bottom line is that PC-ROUTE can perform usable routes. Considering that it is a "first cut" router on a PC, the power of this tool is noteworthy. It works with digital designs, especially smaller designs within the scope of PCB-3. It also can succeed with well-placed analog designs. Both PC-PLACE and PC-ROUTE, however, require significant improvement in their documentation to really unleash their power.

END TO END

PCB-3 is an end-to-end system in a limited sense—limited in that it requires the user to intervene with non-P-CAD tools, or extra design efforts in areas that should be automated for error-free results. These limitations include true GND and PWR plane support, incomplete reference designator support, incomplete power and ground support in digital schematic libraries, special requirements for modification of the back annotation files, incomplete graphics, the lack of direct Gerber support, and inadequate analog support in placement and autorouting. Without the intervention to add necessary changes, it is easy to lose the continuity required of true end-to-end CAD. The documentation, consisting of manuals and charts, examples and lessons, is not up to the caliber of a mature product. The inability to view Gerber data before committing to plot it on film is a particularly unfortunate omission since the film cycle is not usually controlled by the user.

In the final analysis, PCB-3 1.3 is a fairly mature product for a first-generation end-to-end electronic CAD system that works on a PC.

Some of the shortcomings of PCB-3, such as the inability to view part attributes, can be overcome with the use of P-CAD's PDIF product, available at an additional cost. However, the introduction of yet another module into the design cycle may be adding complications to a product that is already intricate.

The security device is a great inconvenience. It is attached to one of the serial ports, but the device is not always transparent to other applications. Sometimes this can be cured by removing the power supply cable and reinserting it. (In a few test instances, even a third security device supplied by P-CAD would not allow any other application to run at all.) It is unsatisfactory to have a copy-protection device so intrusive as to require the disconnection of cables on the back of the unit so that the computer can be used for other purposes.

PCB-3 is not cheap—about $15,000 before the cost of libraries and maintenance is added in. Some other systems cost the same or more. But a very capable crop of under-$2,500 systems is waiting in the wings; of course, they will have to mature, but it may be just a matter of time until they catch this product. Another aspect to consider is that maintenance and support should be included. The P-CAD standard warranty of 90 days includes free updates during that period. For a software product of such complexity, a minimum of two years should be the rule, five years if the company really believes in the product. P-CAD sells a maintenance agreement with the system. Without a corporate discount, the maintenance cost will be about 12 percent of the system cost per year. A maintenance agreement buys priority, high-level BBS access, discounts, and updates during the period. Considering the claims of software performance and quality, the supposed ease of operation, and that PCB-3 is still evolving to meet P-CAD promises, this is a usurious charge.

The training that should be free for such an investment instead costs $2,100 per user (plus hotel and airfare) and takes eight days. The classes are taught at the P-CAD offices, and include instruction on all PCB-3 programs.

P-CAD also needs some improvement in providing good maintenance to purchasers—not in handling customer inquiries or problems, but in notifying users when a program bug is discovered. The bugs are not listed on the user BBS. It would seem that $15,000 should be enough to ensure prompt notification of such problems.

Granted, P-CAD has invested a great deal of time and effort into this product, having spawned many unique and effective capabilities. The package has a lot of CAD ability, and it has maintained its integrated approach throughout its development to date. In the final analysis, PCB-3 release 1.3 is a fairly mature product for a first-generation end-to-end, electronic CAD system that performs on a PC.

PCB-3 1.3: $14,950
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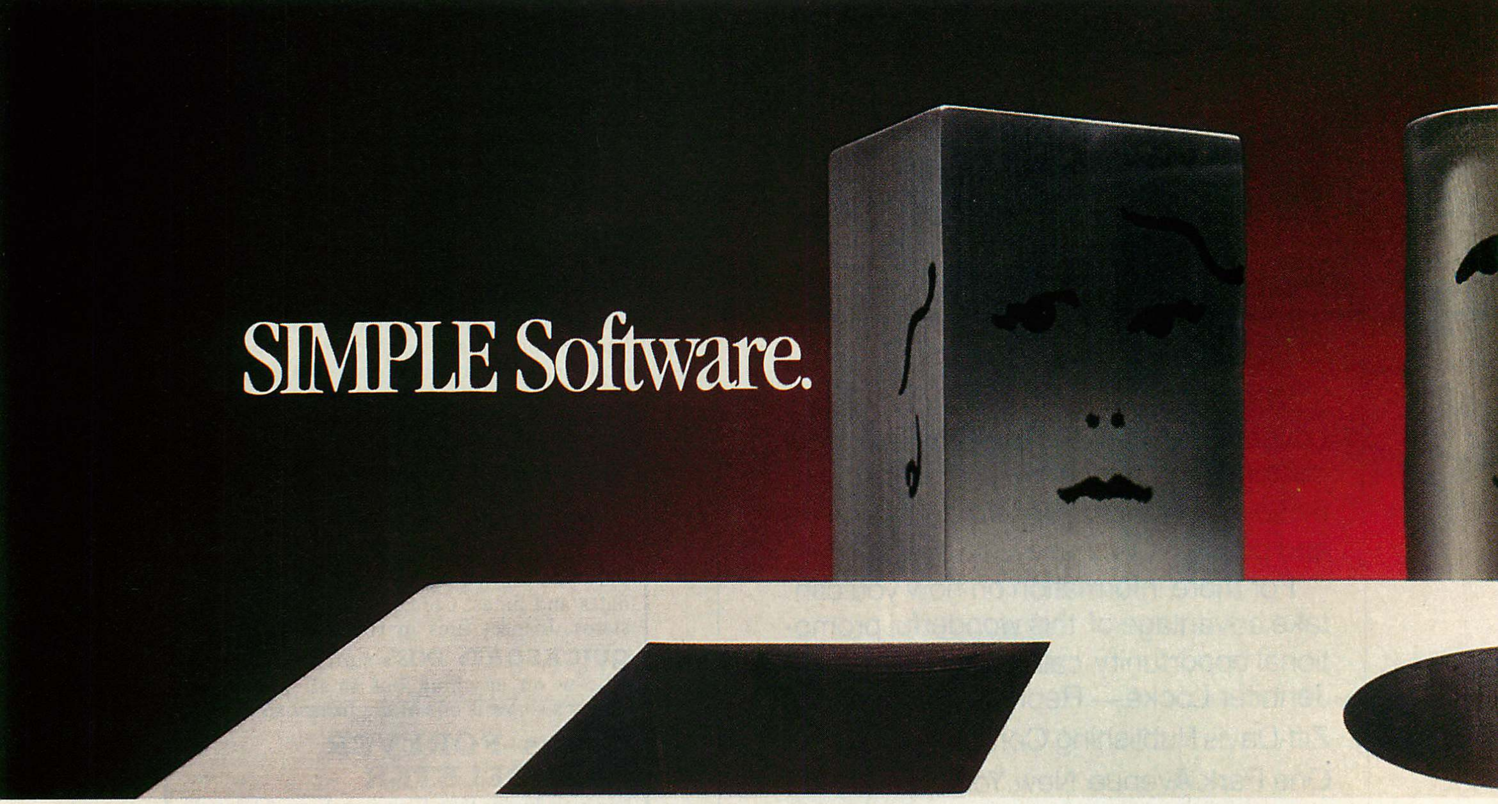
CIRCLE 341 ON READER SERVICE CARD

Richard Angell is the president of Richard Angell Consultants, a firm that specializes in microcomputer CAD applications, operations, and management.



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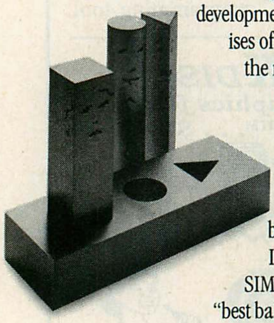

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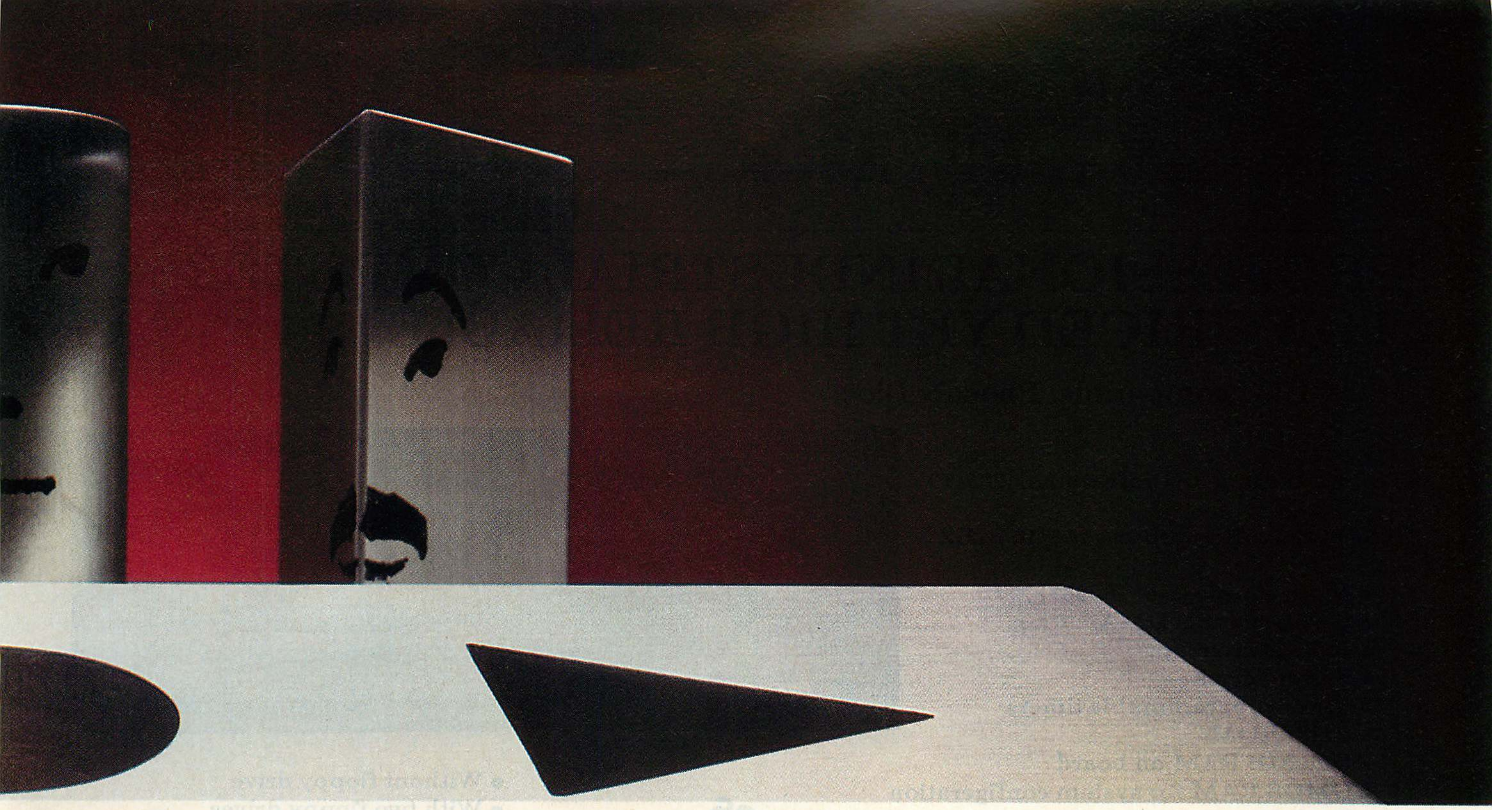
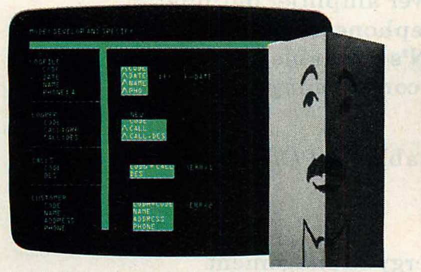
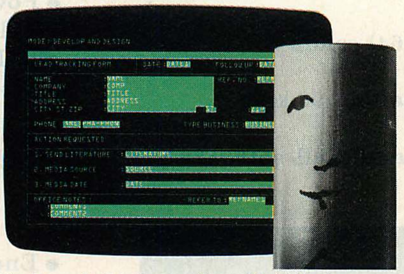


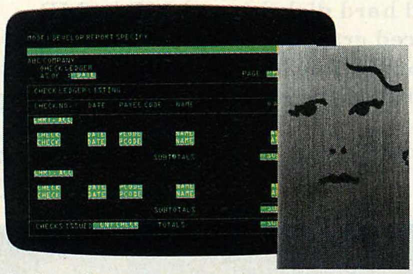
tool for every Tom, Dick and Harriett.



For Example, Company Managers like Tom, Head of Customer Support for a Chain of Retail Outlets, easily develop customized applications. SIMPLE lets Tom develop a Branch Reporting System which reports information from support service calls. Tom wants a system which validates certain information and provides a customer history to improve the branch's support capabilities. With SIMPLE's Specify Worksheet on screen, Tom simply joins data from four different files and establishes their relationship. This enables the user to pull-up call classifications, also verify if the caller has been called on before.



For Example, Information Center Staff Members like Dick, who works for a major Computer Hardware Manufacturer, develop new microcomputer applications systems with SIMPLE. Dick is working with the Director of Marketing on a lead-tracking system. Today, they're reviewing the data entry screens developed with SIMPLE. Dick sits down to review the main data entry screen which shows the prospect demographic information, the media source and date from which the lead was generated, and the fulfillment literature to be sent.



For Example, System Analysts/Programmers like Harriett easily prototype design changes, interacting directly with department heads. Harriett has completed the prototyping with the help of SIMPLE of some previously requested changes in a large Insurance Company's Mainframe Payables System. She has built a test database with data imported from the mainframe and is going to review a check-ledger report in the Controller's office on her portable computer. Harriett shows the Controller exactly how the new system gives a report of all checks issued.

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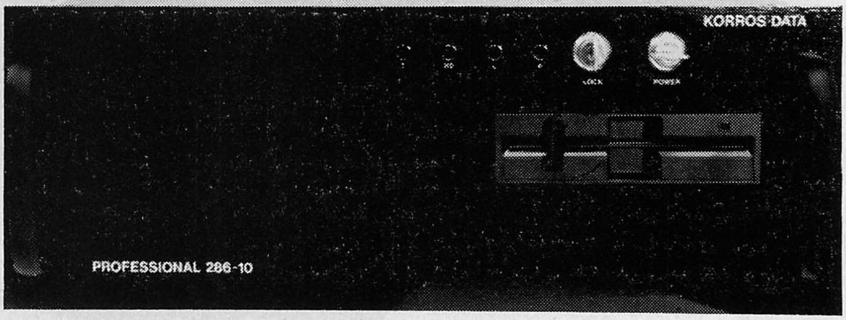

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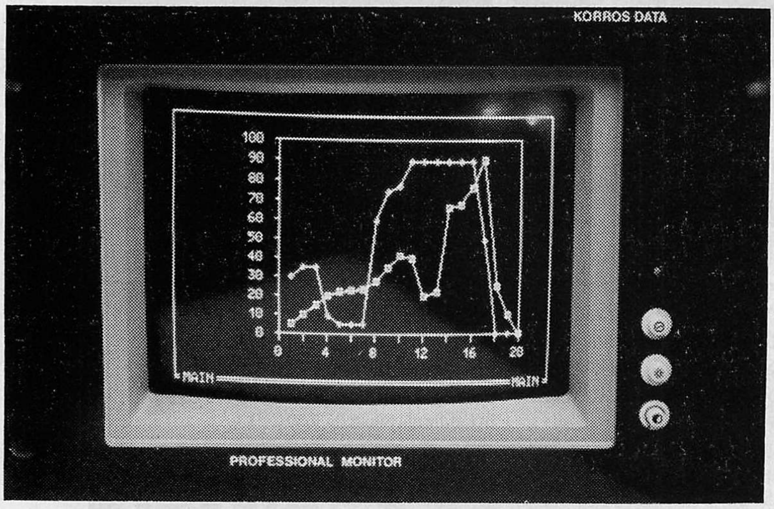

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MARSHALL BRAIN

Jump Searching Linked Lists

A method of jump searching allows programmers to create large, doubly linked lists in Pascal and perform rapid searches.

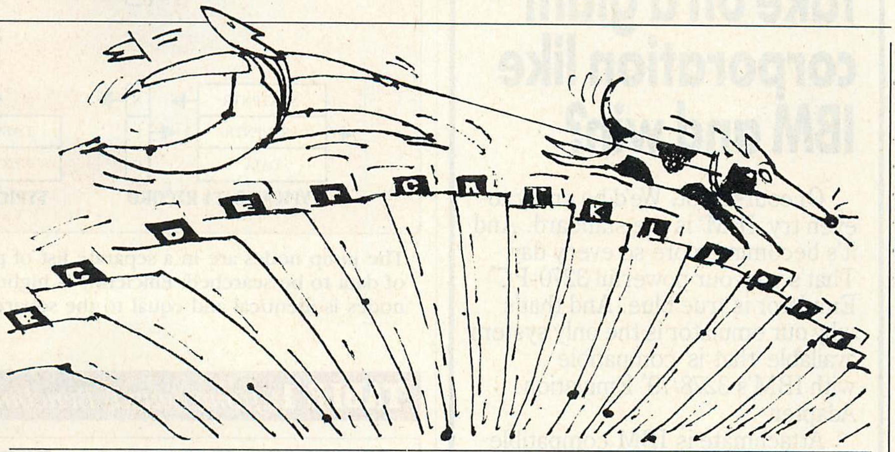


ILLUSTRATION • MACIEK ALBRECHT

When using dynamic variables to store sorted data, programmers often are faced with the dilemma of selecting an efficient storage and search process. They usually arrange the data items in a doubly linked list, because the code to add or delete items in a linked list is simple and fast. Unfortunately, search times for very large lists can become immense and impractical.

When fast searching is needed, programmers frequently choose a B-tree structure. Search times for even the largest tree are short, but the code required to manage insertion and deletion in a tree is bulkier and more difficult to code than that of a linked list. If many insertions and deletions are necessary, the tree becomes unbalanced and search times increase. The time and space needed to balance a tree often negate any speed-up in searching times, thus making trees unsuitable when large numbers of inserts and deletes are taking place.

A solution called *jump searching* can be used with any doubly linked list that contains sorted data. The performance of jump searching falls between that of sequential searching of simple linked lists and searching of trees. The benchmark results summarized in table 1 show jump searching to be an average of 40 times faster than a sequential search of a 10,000-element linked list. The set-up time for jump searching is very short, giving it an edge over trees for lists that are updated frequently.

The theory behind jump searching is simple. Imagine a 10-page list of sorted names. A purely sequential search of this list starts at the first name and then looks at each name on the list one after another. The search ends when the desired name is found, or when the search goes beyond the name in alphabetical order.

Most people do not search this way, however. They usually look at the first name on each page, jumping from page to page until they pass the name they are looking for. Then they back up to the previous page and scan down to find the desired name.

Jump searching works in just the same way. A linked list of *jump nodes* is created with each node acting as an imaginary top of a page. For maximum efficiency in a doubly linked list of **n** items, **sqrt(n)** pages or jump nodes should be created, each holding **sqrt(n)** separate items of the list. If **n**=10,000, there should be 100 nodes with 100 items between each node. A coarse search can be done by jumping from node to node, just as a person goes from page to page. Once the closest node is found, a fine search can be performed on individual data items—at most **sqrt(n)** of them.

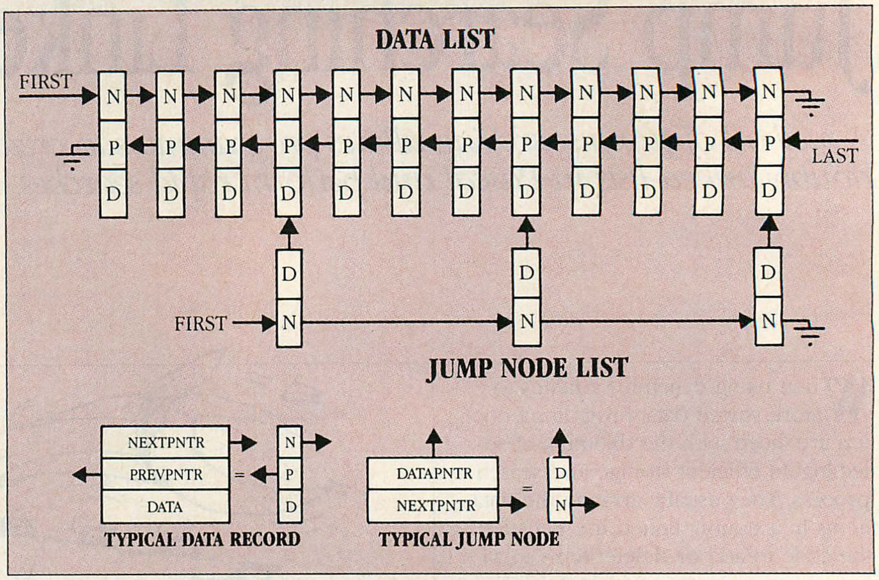
Listing 1 demonstrates the code needed to implement jump searching. The program is comprised of three steps. First, a standard-sorted, doubly linked list is created. The jump nodes are then created so that jump searching can be used. Each node consists of a pointer to an actual data item in the list, as well as a pointer to the next jump node. This structure is illustrated for a 16-item doubly linked list (figure 1).

Once the nodes are created, the list can be jump searched. A coarse search moves from jump node to jump node, examining the data pointed to by the data pointer in each jump node. This is done until a jump node is found that points to a data item greater than or equal to the item to be found (equivalent to being one page beyond the desired item). A fine search then moves backwards through the actual data items, examining each list element in the normal manner until a match is found, or until the search data is discovered to be greater than the list data at the search point.

Once a set of jump nodes has been created, the linked list may be manipulated normally. Insertions are done just as in any doubly linked list. As the list is subjected to more and more insertions and deletions, however, the distance between jump nodes will become unequal and search efficiency for the larger regions between nodes will suffer. This is equivalent to the problem of an unbalanced tree and is remedied in similar fashion—by disposing of the list of jump nodes and generating it anew. As shown in table 1, the amount of time needed for this balancing is quite low.

Deletions are only slightly more complicated. No jump node should point to a specific data item that is being deleted. If it does, the data pointer in the jump node should be moved to an adjacent data item.

FIGURE 1: *Data Structures for Jump Searching*



The jump nodes are in a separate list of pointers linked into the doubly linked list of data to be searched. Efficiency is highest when the distance between the jump nodes is identical and equal to the square root of the number of items in the list.

TABLE 1: *Jump Search Benchmarks*

NUMBER OF ELEMENTS	SEQUENTIAL SEARCH TIME	JUMP NODE SET-UP TIME	JUMP SEARCH TIME	SPEED-UP FACTOR
100	.11	.05	.05	2.2
500	1.43	.11	.22	6.5
1,000	5.55	.17	.44	12.6
5,000	138.20	.55	4.89	28.2
10,000	552.86	.93	13.74	40.2
13,000	929.56	1.15	20.16	46.1

All times are in seconds. Tests run on an IBM PC with 640KB of RAM.

The time required to create the linked list of jump nodes (equivalent to rebalancing a B-tree) is negligible compared to the time required to perform the search, and could conceivably be performed before every search of a large list.

A jump search on a list of 10,000 elements would take, on the average, 100/2=50 examinations using jump nodes and then another 50 examinations of actual data items, for an average of 100 examinations. A purely sequential search would take an average of 10,000/2=5,000 examinations to find any data item. A balanced binary tree would take $\log_2(10{,}000)$, or approximately 14 examinations. The balancing time for very large trees can be quite long, however, and when trees are modified frequently, they become unbalanced very quickly.

Table 1 shows benchmarks comparing sequential-searching times with jump-searching times for variously sized lists. The table was created using the code in listing 1. This code creates a doubly linked list; each element in the list contains an integer. The integers start at 1 and increase by 1 to the total number of elements on the list. This doubly linked list is then searched, looking for every 11th item. For example, in the case of a 100-element list, 100 elements are created, each sequentially containing the numbers between 1 and 100. The program then searches for the numbers 1, 12, 23, . . . 100. The timings indicated that for large lists, jump searching is a significant improvement over sequential searching and close enough to B-tree searching to be worthy of consideration.

Marshall Brain, a graduate student in computer studies, is an instructor at North Carolina State University in Raleigh.

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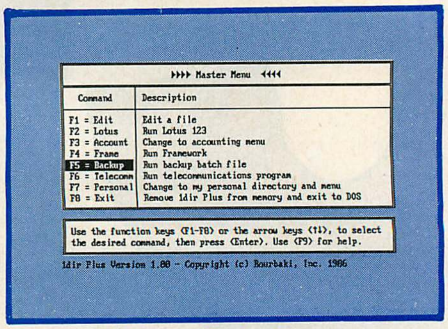
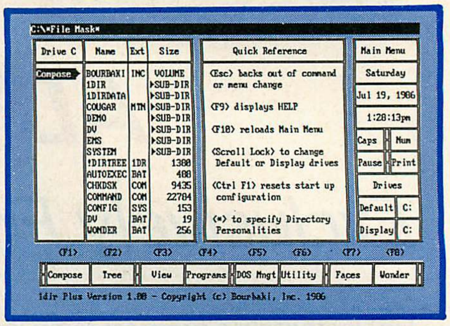
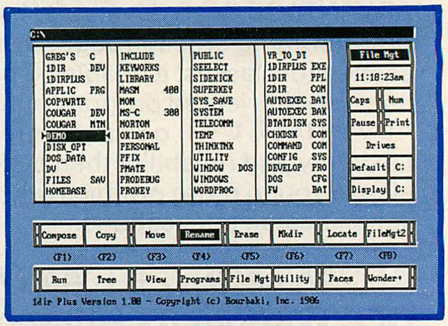


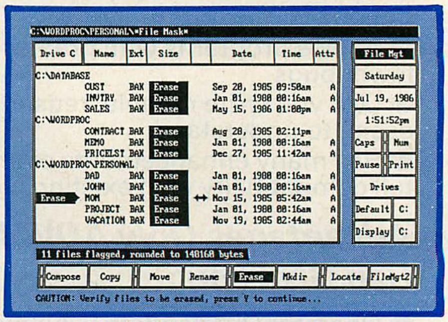
Menu Only Face



Quick Reference Face



Two Menu Face



Global Directory Face

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LISTING 1: JUMPSRCH.PAS

```
program Jump_search;
{$u-,r-,k+,c-}
{ Marshall Brain       July 17, 1986
  This program implements the Jump Search algorithm.}

type
  num_pntr=^data_rec;
  jump_pntr=^jump_rec;

  {typical data record - forward and backward pointers and data}
  data_rec=record
    nextpntr,prevpntr : num_pntr;
    num  : integer;
  end;

  {A Jump Node consists of a single link forward and a
   pointer to a specific data item.}
  jump_rec=record
    nextjump:jump_pntr;
    data_pntr:num_pntr;
  end;

var
  tempdata,firstdata,lastdata:num_pntr;
  tempjump,firstjump,lastjump:jump_pntr;
  prevtimecx,prevtimedx,timedx,timecx:integer;
  list_size:integer;
  time:real;

  procedure fill_data_list;
  {creates a double linked list of list_size elements on the
   heap. Each record on the heap contains 2 pointers and the
   "data", it this case a single integer.}
  var x:integer;

    procedure append_to_list;
    {appends the next data record to the end of the list. In a normal
     program this would be replaced by insertion and deletion
     routines for the linked list.}
    begin
      {if no records in list, then make current record the first.}
      if firstdata=nil then
      begin
        firstdata:=tempdata;
        lastdata:=tempdata;
        tempdata^.nextpntr:=nil;
        tempdata^.prevpntr:=nil;
      end
      {otherwise append to end of list.}
      else
      begin
        lastdata^.nextpntr:=tempdata;
        tempdata^.nextpntr:=nil;
        tempdata^.prevpntr:=lastdata;
        lastdata:=tempdata;
      end;
    end;

  begin {fill_data_list}
    firstdata:=nil;lastdata:=nil;
    {This demo uses simple data in the linked list - a set of
     consecutive integers. Note that list MUST be sorted to use
     the jumping technique.}
    for x:=1 to list_size do
    begin
      new(tempdata);
      tempdata^.num:=x;
      append_to_list;
    end;
  end;

  procedure create_jump_list;
  {Given a sorted linked list, this routine will create a balanced
```

```
  jumping list to use for searching.}
 var y,x,jump_distance:integer;

   procedure create_jump_node;
   {creates and links in a new jump node.}
   begin
     new(tempjump);
    {point jump records data pointer at current data item.}
     tempjump^.data_pntr:=tempdata;
    {form linked list of jump records by appending onto end of
     jump list.}
     if firstjump=nil then
       firstjump:=tempjump
     else
       lastjump^.nextjump:=tempjump;
     tempjump^.nextjump:=nil;
     lastjump:=tempjump;
   end;

  begin {create_jump_list}
   {determine optimal jump distance.}
    jump_distance:=trunc(sqrt(list_size));
    x:=1; y:=1;
   {start with first element of data list.}
    tempdata:=firstdata;
    firstjump:=nil; lastjump:=nil;
   {sequence through entire list.}
    while y<list_size do
    begin
      {every sqrt(list_size) create a jump node.}
      if x>=jump_distance then
      begin
      create_jump_node;
      x:=0;
    end;
   {get next data item in list.}
    tempdata:=tempdata^.nextpntr;
    y:=y+1; x:=x+1;
   end;
  {create final jump node at very end of list.}
   create_jump_node;
end;

procedure jump_search(num_to_find:integer);
var found:boolean;

  procedure coarse_search;
  {the coarse search jumps through the jump nodes looking for
   the nearest match to the data to be found. As soon as a
   jump node is found pointing to a data item >= the item
   to be found, the course search stops.}

  var done:boolean;

  begin
   {start at first jump node.}
    tempjump:=firstjump;
    done:=false;
    while not done do
    begin
     {stop when data item >= num to be found.}
      if tempjump^.data_pntr^.num>=num_to_find then
        done:=true
      else
      begin
        {Also stop course search at end of jump list (last
         element in data list).}
        if tempjump^.nextjump=nil then
          done:=true
        else
          tempjump:=tempjump^.nextjump;
      end;
    end;
  end;

  procedure fine_search;
  var stop:boolean;
  {fine search then goes backwards thru every element in data
   list itself until item is found or item can not exist.}

  begin
   {start looking at jump node coarse search stopped at.}
    tempdata:=tempjump^.data_pntr;
    found:=false; stop:=false;
    while not found and not stop do
    begin
     {if beyond possibility, stop search.}
      if num_to_find>tempdata^.num then
        stop:=true
      else
      begin
        if num_to_find=tempdata^.num then
          found:=true
        else
          tempdata:=tempdata^.prevpntr;
      end;
    end;
    if not found then write(' not found ');
  end;

begin {jump_search}
  coarse_search;
  fine_search;
  {at this point programmer decides what to do with the found data
   item. FOUND will be true if found, and TEMPDATA will point to
   found data item.}
end;

procedure sequential_search(num_to_find:integer);
{standard sequential search routine used
 for comparison in benchmarking.}

var stop,found:boolean;

begin
  tempdata:=firstdata;
  found:=false; stop:=false;
  while not found and not stop do
  begin
    if num_to_find<tempdata^.num then
      stop:=true
    else
    begin
      if num_to_find=tempdata^.num then
        found:=true
      else
        tempdata:=tempdata^.nextpntr;
    end;
  end;
end;

procedure beep;
begin
  sound(500);
  delay(1000);
  nosound;
end;

procedure get_time(var cx,dx:integer);

var result:record ax,bx,cx,dx,bp,si,di,ds,es,flags:integer; end;

begin
  result.ax:=0;
  intr($1a,result);
  cx:=result.cx;dx:=result.dx;
end;

procedure calc_time;
begin
  time:=(timecx-prevtimecx)*65536.0 +
```

```
    (hi(timedx)-hi(prevtimedx))*256.0 +
    (lo(timedx)-lo(prevtimedx));

  time:=time/18.2;
end;

procedure time_searches;

var a:integer;jtime:real;

begin
  write('  Jump Searching list.        ');
  get_time(prevtimecx,prevtimedx);
  a:=1;
  while a<=list_size do
  begin
    jump_search(a);
    a:=a+11;  {use prime number to avoid bias in benchmarks.}
  end;
  get_time(timecx,timedx);
  calc_time;
  writeln('    done. Time =',time:6:2);
  jtime:=time;
  writeln;
  write('  Sequentially Searching list.');
  get_time(prevtimecx,prevtimedx);
  a:=1;
  while a<=list_size do
  begin
    sequential_search(a);
    a:=a+11;  {use prime number to avoid bias in benchmarks.}
  end;
  get_time(timecx,timedx);
  calc_time;
  writeln('    done. Time =',time:6:2);
  writeln;
  if jtime=0 then jtime:=0.05;
  writeln('Jump Searching was ',time/jtime:4:1,
         ' times faster for a ',list_size,
         ' element list');
end;

procedure setup;

var error:boolean;

begin
  clrscr;
  gotoxy(1,5);
  writeln
  ('This program will produce a benchmark comparing the time to');
  writeln
  ('do a number of sequential searches with a number of identical');
  writeln
  ('Jump Searches. You will be asked to enter a number indicating');
  writeln
  ('the number of elements to be placed in the linked list used');
  writeln
  ('for this test.  Numbers greater that 1000 can produce very');
  writeln
  ('long sequential searches in this test, but results are');
  writeln('more dramatic for longer searches.');
  writeln;
  writeln('Enter the number of items to be in the linked list.  ');
  write('Please type an integer less than 30000 : ');
  readln(list_size);
  writeln;writeln;
end;

procedure make_linked_list;
begin
  writeln;
  writeln('List size for test = ',list_size);
  writeln('Number of searches for test = ',list_size div 11);
  writeln('All times are in seconds.');
  writeln;
  writeln('  Setting up linked list used for testing.');
  fill_data_list;
  writeln;
end;

procedure make_jump_list;
begin
  write('  Creating Jump Nodes.        ');
  get_time(prevtimecx,prevtimedx);
  create_jump_list;
  get_time(timecx,timedx);;
  calc_time;
  writeln('    done. Time =',time:6:2);
  writeln;
end;

  function size_ok:boolean;

  var x:real;

  begin
    if maxavail<0 then x:=maxavail+65536.0 else x:=maxavail;
    if x*16.0-(list_size*16.0+trunc(sqrt(list_size))*8.0)<0.0 then
      size_ok:=false
    else
      size_ok:=true;
  end;

begin {main}
  setup;
  if size_ok then
  begin
    make_linked_list;
    make_jump_list;
    time_searches;
    beep;
  end
  else
    writeln('Linked list created would be too large',
           ' for your available memory.');
end.
```

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CIRCLE NO. 246 ON READER SERVICE CARD

Reviews and Updates

LOGIMOUSE C7
Logitech, Inc.

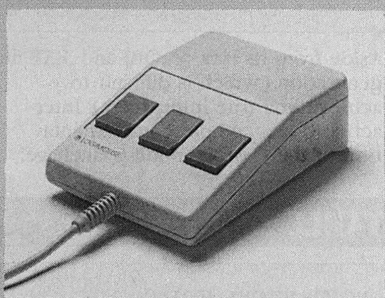
INTERACTIVE-C 1.41
Impacc Associates

PC TOOLS 2.03
Central Point Software

LOGIMOUSE C7

Logitech, Inc.
805 Veterans Blvd.,
Redwood City, CA 94063
415/365-9852

PRICE: Basic $99; Plus $119



CIRCLE 342 ON READER SERVICE CARD

Logitech's Logimouse C7 is a three-button, mechanical-optical serial mouse for the PC. The $99 basic package reviewed here includes the mouse, driver software, test program, and interface source code for Turbo Pascal, Microsoft C 4.0, and Logitech's own Modula-2 compiler. Several optional software packages are available at a discount along with the Logimouse, including Generic CADD 2.0 (Generic Computer Systems), PC Paintbrush (Z-Soft Corp.), and Reflex (Borland International). Logitech also offers a "Plus" package that includes a menuing utility and a multiwindow text editor.

In many ways, the Logimouse represents a melding of the best features of both its major competitors, the Microsoft Mouse and the Mouse Systems PC Mouse. The optical PC Mouse, with no moving parts, would seem to have an edge in reliability, but the precision-ruled optical pad is vulnerable to scratches. Furthermore, because it must provide continuous light, the PC Mouse cannot be run on power "stolen" from a serial port; a power supply and attendant cabling are required.

Unlike the Microsoft Mouse's entirely mechanical technology, the Logimouse incorporates a hybrid optical/mechanical design: a rubber-coated metal ball runs in an enclosed race, from which the ball can be easily removed without tools for cleaning. The ball turns against two perpendicular wheels connected to optical encoders that emit streams of pulses at a rate proportional to their rotation. Both mice incorporate low-power CMOS logic that can be run from power extracted from the signal lines of an RS-232 serial port.

Ergonomically, the Logimouse and the PC Mouse are very close; both have three-buttons and a flat, wide rectangular shape compared with the thicker, narrower Microsoft Mouse. Unlike the Microsoft Mouse, the Logimouse and the PC Mouse can be manipulated largely by the weight of the hand resting atop them; very little gripping is required. This becomes important when using a mouse-based graphics package for hours at a stretch.

Good mouse switches, like good keyboard switches, provide a positive, tactile snap action that indicates actuation of the switch. The Logimouse switches are very good—much better than the Microsoft Mouse's—but they feel slightly tight and bulky compared with those of the PC Mouse.

Like the Microsoft Mouse 2.0, the Logimouse is capable of resolving 200 lines per inch, whereas the PC Mouse is still limited to 100. The alignment of the sensors in a pad-style optical mouse becomes critical when the resolution climbs above 100 lines per inch; dropping an optical mouse with a higher resolution can misalign the sensors sufficiently to render it inoperative.

Logimouse software support is excellent. Three drivers are supplied: a resident driver run as a .COM file; a DOS installable device driver; and a Microsoft Windows driver in .DRV format. (The Windows driver is not necessary because current versions of Windows are shipped with the Logimouse driver on the set-up menu.) The current release of the driver implements all Microsoft Mouse driver 2.0 function calls through interrupt 33H. Earlier releases of the Logitech driver included nine proprietary function calls implementing extended mouse functions, but these were dropped to avoid incompatibility with what has come to be a de facto mouse interface standard.

The Logimouse is currently offered as a serial port device only. (The Microsoft Mouse is also available with a PC bus interface as a short card.) Its resident and DOS device drivers support either COM1 or COM2, specified when the driver is installed. Unlike the PC Mouse under Windows, the Logimouse does not require the user to specify which serial port will support the mouse when the Windows driver is installed; the driver automatically polls both ports when Windows initializes. This ability should be propagated to Logitech's non-Windows drivers as well.

Without any driver installed, the Logimouse is operationally identical to the PC Mouse. This was tested by installing both GEM (Digital Research, Inc.) and Microsoft Windows for the PC Mouse and then replacing the PC Mouse with the Logimouse; operation continued unchanged. The Logimouse driver functions with most current applications requiring mouse support. This compatibility was tested by running Logimouse with Reflex, Windows, GEM, Microsoft QuickBASIC 2.0, EGA Paint (RIX SoftWorks, Inc.), and Dr. Halo DPE (Media Cybernetics), all configured for the Microsoft Mouse. No differences in operation were observed.

One additional feature that would be very desirable is the ability to operate through serial ports beyond COM1 and COM2. Multiple serial port boards have become fairly common (see

"Beyond COM2," Augie Hansen, September 1986, p.68) and future mouse drivers should address the use of these additional serial ports.

The Logimouse documentation is well-organized and crisply written. Only about 25 pages of text, however, describe the mouse, its installation, and its use in the basic package. The remainder is devoted to the utilities and text editor provided with the Logimouse Plus package. The documentation fails to clearly distinguish the Plusus package from the basic package.

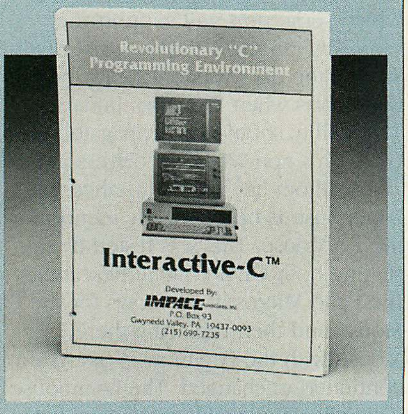
The Logimouse is a mature product: rugged, reliable, and well-supported. With a strong software standard in place, the choice between the Microsoft Mouse and the Logimouse comes down to one of aesthetics (the number of buttons, the feel of the switches, and shape of the case). Finally, there is price: at $99 retail, the Logimouse is the least expensive mouse that is currently offered, by a major vendor. If a serial port can be committed to its use, Logimouse C7 comes highly recommended.

—JEFF DUNTEMANN

INTERACTIVE-C 1.41

Impacc Associates
P.O. Box 93,
Gwynedd Valley, PA 19437
215/699-7235

PRICE: $249



CIRCLE 343 ON READER SERVICE CARD

Like other C interpreters, Interactive-C from Impacc Associates exploits its interpreted architecture to improve the convenience and safety of creating new C code. At the core of its program development and debugging environment is a source interpreter, holding code in memory in tokenized form in a fashion similar to IBM BASICA. Impacc claims its product supports the full C language with no restrictions, even in the normally troublesome (for an interpreter) preprocessor; testing has borne this out. The product requires about 250KB of disk space, allowing use from a diskette, and will operate in a PC with 256KB. The basic specifications for Interactive-C are shown in table 1. (Interactive-C arrived too late for inclusion in *PC Tech Journal*'s review of C interpreters, "The State of C Interpreters," Marty Franz, May 1986, p. 153.)

Installation is not difficult. A configuration file is used to specify the type of display, the memory to allocate for functions and variables, and the limits of stack safety checking.

In operation, Interactive-C provides the programmer with four windows: for program output, editing, commands, and status. The program output window can be rerouted to a separate video adapter card and monitor for dual-screen debugging. With a single monitor, the FLIP command is used to switch the display between the program being debugged and Interactive-C.

Interactive-C supports the Lattice C library and "standard" (table 3). In fact, the interpreter itself is written in Lattice C. The large model is used, meaning that PCs with 640KB of RAM can be used to develop sizable programs given the interpreter's modest memory requirements (smaller than many new BASICs). New library functions can be added by compiling and linking them with an external library table module, XLIBDIR.C. This obviates the need to source-interpret library functions.

As table 3 shows, the editing facilities provided by Interactive-C are basic and sure to disappoint experienced programmers, who are used to having extras such as macro processors and multiple text windows. The editor is driven by the function keys and has the ability to edit multiple buffers. Only 16 lines of text can be displayed at any one time; the remaining lines of the screen are occupied by the interpreter's command and status windows.

Interactive-C has excellent debugging facilities as shown in table 3, including the ability to stop a program, alter its code, and resume execution. Variables also may be altered during execution from the debugger. Any legal C expression or library function may be executed from the debugger in immediate mode; however, functions contained by the program being interpreted may *not* be executed from the debugger. The editor and debugger are tightly coupled; moving between the two facilities is easy and intuitive.

TABLE 1: *Features*

Version tested	1.41
Disk space (KB)	250
RAM required (KB)	256
Full K&R language	●
Standard library	●
PC-specific library	●
Sample programs	●
Library source code	●
Memory model	Large
Editor	●
Debugger	●
Loadable libraries	●
Assembler interface	●
.OBJ output	○
.EXE output	○

● = Yes ○ = No

These features can be compared with those for other C interpreters in table 1 in "The State of C Interpreters" (Marty Franz, May 1986, p. 154).

Aside from its lack of .OBJ and .EXE file generation (which is difficult to achieve in a true interpreter), Interactive-C is a complete implementation of the C programming language.

TABLE 2: *Library Features*

UNIX STANDARD LIBRARY	
Stream files	●
Ato?? conversions	●
Ito?? conversions	●
Str?? functions	●
Random files	●
Memory management	●
Setjmp( )/longjmp( )	○
PC-SPECIFIC	
Bdos( )	●
Int86( )	●
Interrupt handler	○
Segread( )	●
Communications	○
ADDITIONAL	
Math	○
Trig	○
Graphics	○
Sound	○
LIBRARY	
Availability	Good

● = Yes ○ = No

These library features can be compared with those for other C interpreters in table 3 in "The State of C Interpreters" (Marty Franz, May 1986, p. 156).

External libraries may be loaded if they are in the Lattice large model format. As many such libraries are available, this compensates for Interactive-C's lack of built-in support for graphics, sound, and other advanced I/O features.

TABLE 3: *Editing and Debugging Facilities*

EDITOR	
Full screen	●
Paging	●
Insert/overlay	●
Search/replace	●
Block move/copy	●
Multiple buffers	●
Automatic format	●
Shell facility	●
Go to last error	●
DEBUGGER	
Trace	●
Breakpoint	●
Single step	●
Side Step[a]	●
Pointer check	●
Display variables	●
Display memory	○
Alter variables	●
Alter program	●
PROGRAM PROFILER	○
SIDEKICK COMPATIBLE	●

● = Yes ○ = No

[a]*Single steps code but executes function calls at full speed*

These features can be compared with those for other C interpreters in table 4 in "The State of C Interpreters" (Marty Franz, May 1986, p. 157).

Interactive-C's lack of an execution profiler is not a serious deficiency because the performance of the interpreted code is too slow to make profiler optimization worthwhile.

TABLE 4: *Benchmarks*

SIEVE.C	125.03
FILECOPY.C	5.54
PENTATH.C	
Floats	46.62
Functions	234.82
Strings	173.24
Chars	24.63
Files	492.05
Makefile	410.99

All times are in seconds. Timings were taken on a dual diskette drive IBM PC with 512KB of RAM running under DOS 2.1.

These benchmark times can be compared with those for other C interpreters in table 6 in "The State of C Interpreters" (Marty Franz, May 1986, p. 159).

Interactive-C's performance is on a par with other true C source interpreters, but it is slow compared to the C compilers that are customarily used in program development. Its rapid prescanning of the programs before running them serves to improve performance.

It is not well documented and not controllable by the user, but safety checking is performed on pointers. Any pointer reference outside the code or data areas will be intercepted and disallowed. Because this slows pointer operations down noticeably, it would be useful to disable pointer safety checking when program development is complete. Interactive-C includes the ability to set the program's stack size and specify a "warning area" that indicates when the stack is near exhaustion. Overrunning the stack is a common error, so this feature aids in debugging.

Interactive-C has two major drawbacks that must be weighed carefully by the prospective user. First, it is a source interpreter, and as a result, it performs poorly relative to intermediate or native code compilers (as the table 4 benchmarks indicate). This execution penalty is offset somewhat by Interactive-C's rapid prescanning of the program before it is run; movement between the editor and program execution is much

TABLE 5: *Documentation*

Installation	Good
Set-up	Good
Tutorial	Poor
Editor	Fair
Error messages	Good
K&R differences	Fair
Library reference	Poor
Linking externals	Fair
Assembler information	Poor
Technical details	Poor
Source code	Poor
Updates	Fair
Index	N/A
Overall rating	Poor

These ratings can be compared with those for other C interpreters in table 5 in "The State of C Interpreters" (Marty Franz, May 1986, p. 159).

There is no rating for the index because there is none. Documentation is Interactive-C's greatest weakness.

faster than in several of the other interpreters. As a great deal of such movement occurs during interactive program development, perceived performance in actual debugging situations is not as bad as the benchmark times indicate.

The Interactive-C documentation is sparse and often confusing (table 5). An index is a necessity for a program of this complexity, and Interactive-C's manual lacks not only an index but also a clear organization. For example, nowhere is a list of the standard functions included in the "internal library." No examples are provided in the function reference section. The manual also lacks technical information: a scant five pages describe the assembly language interface and the linking of external libraries to user code, and no examples are provided of either.

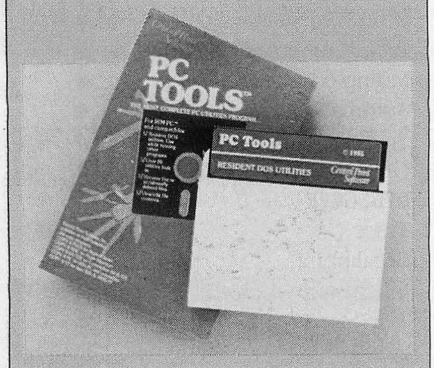
Like most C interpreters currently on the market, Interactive-C falls between being a true C tutorial for beginners and a true C development tool for veteran programmers. Newcomers to C programming are better off with Computer Innovations' Introducing C, and fast interactive development can be done with a true native code compiler/interactive development environment, such as Mark Williams' Let's C, and at a much lower cost. Although technically sound and bug-free, Interactive-C needs better documentation and improved performance before it can be used by serious C developers.

—MARTY FRANZ

PC TOOLS 2.03

Central Point Software
9700 SW Capitol Highway,
Suite 100, Portland, OR 97219
503/244-5782

PRICE: $39.95



CIRCLE 344 ON READER SERVICE CARD

PC TOOLS is a memory-resident disk utility program with powerful, DOS-like features, such as the ability to copy, rename, and delete files. It also can be used to recover erased files, view the contents of files, and find specific text. All of these features can be brought to life at any time by pressing Ctrl-Esc from within another program.

The power implied by this program's concept is impressive. Having DOS utility services available at all times (and only a keystroke away) is quite convenient. For example, PC TOOLS would allow a user to copy a file from the hard disk while the computer is in the middle of a lengthy process that cannot be stopped indiscriminately.

The 68-page booklet supplied with PC TOOLS is well organized and written. Installation was accomplished with no difficulty. However, depending on the number of subdirectories a hard disk has, the user may need to vary the suggested command line parameter that specifies how much memory to set aside for PC TOOLS' use. This memory consumption can be set from 64KB to 136KB or more. For disk systems with many subdirectories, allocating sufficient memory is critical in determining whether PC TOOLS will work at all.

At installation, PC TOOLS builds an overlay file that it will draw upon from time to time. If a system contains expanded memory, PC TOOLS uses that instead for its overlay information, which improves performance but does not reduce the DOS memory requirements.

The initial PC TOOLS screen is called the File Functions menu, which offers these options: compare, copy, delete, move, print, rename, verify, view/edit, find a string of text within selected files, change a files attribute, and print or sort the directory.

PC TOOLS' second main menu, Disk and Special Functions, is accessed with the F3 key. This menu provides these diskette functions: copy, compare, find, rename, verify, view/edit, map, locate, and format. Also within this menu is access to undelete, a file recovery service. A directory maintenance submenu provides functions to rename, create, and remove directories and to change the current directory.

PC TOOLS displays a graphical representation of a hierarchical directory structure called *tree display*. The user can turn a subdirectory into the current subdirectory simply by pointing to it with the cursor. This could be an exceptionally powerful tool, but it is flawed; for example, on a system with 340 subdirectories, PC TOOLS stumbled while drawing the subdirectory interrelationships, positioned the cursor at random places on the display, drew lines where they should not have been, and finally locked up the PC. Central Point said this problem will be corrected with the next release.

An interesting attribute of PC TOOLS is its ability to relocate subdirectories (along with their child directories) to any other subdirectory not contained within itself. Files are not physically moved from place to place on the disk; all moves are accomplished by moving subdirectory entries only. The point-and-shoot interface described above makes the operation virtually effortless.

PC TOOLS may be too powerful for the typical user, because it is easy to get into serious trouble. For example, if PC TOOLS is invoked from within a program that is using files on which PC TOOLS operates, then the suspended program could fail, resulting in a loss of data.

Generally, PC TOOLS does what it claims to do, and aside from the subdirectory capacity bug, it is reliable. Its most serious weakness is the user interface, which lacks consistency and any semblance of careful design. Confirmation is requested for many commands, but the confirmation keys are not consistent from command to command. Screen design is very congested, particularly the help text at the bottom of each screen. With attention paid to user interface, PC TOOLS could become as easy to use as it is powerful.

—GUY QUEDENS

Programming for AI

Although they require unlearning traditional programming techniques, LISP and Prolog are tailored for developing artificial intelligence applications.

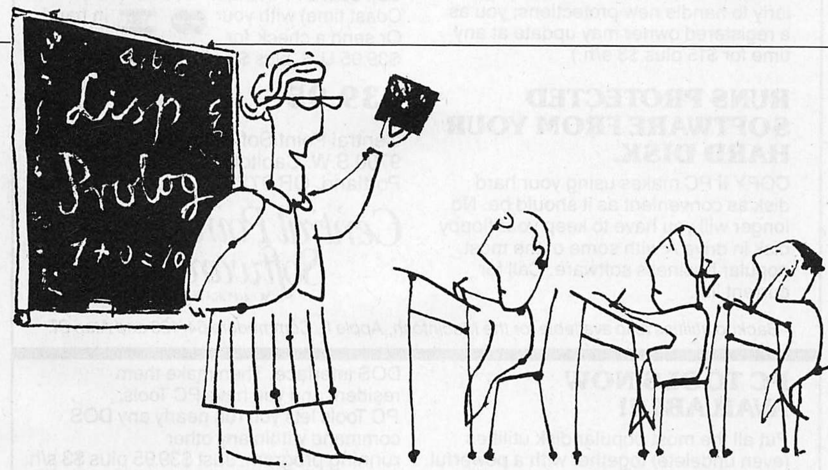


ILLUSTRATION • MACIEK ALBRECHT

In any discipline, the tools of the trade are usually customized to support the most common needs. In the artificial intelligence community, this process has led to development of specialized programming languages. Since the early 1960s, quite a few AI languages have been designed and implemented. Most of these—AMBIT, COGENT, COMIT, DYSTAL, FLIP, FORMAC, IPL-V, SLIP, and TRAC—were experimental and never developed much of a following. Two in particular, LISP and Prolog, have evolved into the most widely used languages for AI programming.

Both LISP and Prolog are general-purpose languages that contain a rich set of primitive functions and operations. PC versions have primitives to control screen input/output, read and write files, issue BIOS calls, and even call functions written in other languages. This column will address AI languages and the techniques they support, especially concentrating on the central ideas that distinguish LISP and Prolog from other computer languages.

A key aspect of AI languages is that they support rapid prototyping of experimental systems. In fact, certain LISP implementations offer complete development environments rather than simple compilers. Interactive editors and debuggers, performance monitoring tools, graphics packages, and version management software are often included within the environment. AI languages tend to be interpretive, allowing programmers to debug a program quickly in an interactive mode, then compile for speed afterward.

SYMBOL MANIPULATION

The primary emphasis of AI languages is on *symbol manipulation*, as opposed to "number crunching." Symbol manipulation can be described with the following analogy. Consider the difference between arithmetic and algebra. Arithmetic concerns itself only with computations on numerical data. Algebra, though, involves manipulations of symbols—moving variables from one side of an equation to another, factoring, and so on, according to certain rules.

Nearly all AI research concerns itself primarily with pushing symbols around—from controlling robots to playing chess. For this reason, all AI languages provide special support for symbol manipulation. This support has several key aspects, listed below.

Nonnumeric data types. Besides the usual support for numbers and strings, AI languages offer direct ways of building symbolic data structures, such as trees and sequences of symbols. For example, the LISP construct

```
(RED GREEN YELLOW)
```

denotes a list of the symbols RED, GREEN, and YELLOW.

Typically, automatic support is provided for allocating memory to store symbolic objects and for giving the memory back to a central pool when the user is done with the object. This "garbage collection" mechanism obviates the need for explicit allocation and freeing of storage (such as with the **alloc** and **free** functions in C).

In some AI languages, programmers can manipulate programs in the same way data are manipulated—in fact, programs are considered to be data for some purposes and are stored as lists.

Pattern matching. Much of AI problem solving is concerned with searching a large space of possibilities for certain patterns. A number of early symbol manipulation languages, such as SNOBOL, AMBIT, and COMIT, provided special features for this purpose. The tradition continues with Prolog, which directly supports a special pattern-matching algorithm called *unification*.

Recursion. A program that calls itself as a subroutine is said to be recursive. Recursive algorithms are ubiquitous in AI applications, because the data structures they operate upon tend to be tree-like and, therefore, easily described in a recursive manner.

As an example, suppose L represents a sequence of symbols, such as (A B C). Two functions, **First** and **Rest**, are defined, each of which takes a list as an argument. **First(L)** computes the first symbol in L, and **Rest(L)** computes the list that remains when **First(L)** is removed. Thus, if L = (A B C), then

First(L) = A

and

Rest(L) = (B C)

Now, suppose a function is to be defined that determines whether a

given symbol **A** occurs in list **L**. A recursive function **Member** can be written as follows (**Empty( )** is assumed to be a built-in function that tests whether a given list has any symbols in it at all):

```
Member (A,L) =
  if (Empty (L))
    then FALSE
    else
      if (A = First (L))
        then TRUE
        else Member (A, Rest (L))
```

Note the recursive call on the last line. The algorithm takes advantage of the fact that every list can be recursively decomposed into its **First** and **Rest** parts. This style of divide-and-conquer recursive decomposition is the cornerstone of programming in LISP and Prolog.

Backtracking. It involves trying what seems like a promising path, only to discover that it leads to a dead end. When this happens, the only alternative may be to undo what's been done and try a different path. This process, called *backtracking*, is a very common aspect of AI problem solving, and one for which Prolog provides direct support.

LIST PROCESSING

LISP (for list processing) originated at MIT in the early 1960s and is in widespread use in the AI community. Most of the early work in expert systems, mathematical theorem provers, and natural language-understanding programs was done in LISP. (See "Creating a Standard LISP," Mark Bridger and John Frampton, December 1985, p.98.)

Programs and data are represented in LISP as lists, such as

```
(A B C)
(A (B C))
(+ 1 2)
```

Lists can contain numbers, symbols, or even other lists. The simplest list is the empty list, designated as NIL. The function CAR applied to a list returns the first element of the list, while the function CDR returns the rest of the list. CAR is the analog of the **First** function and CDR is the analog of the **Rest** function that was mentioned earlier.

Function application in LISP is itself written as a list where the first element is the name of the function and is followed by the arguments to the function. Ignoring for a moment the use of the apostrophe, consider the following:

```
(CAR '(A B C))               -> A
(CDR '(A B C))               -> (B C)
(CAR (CDR '(A (B C)) ))      -> (B C)
```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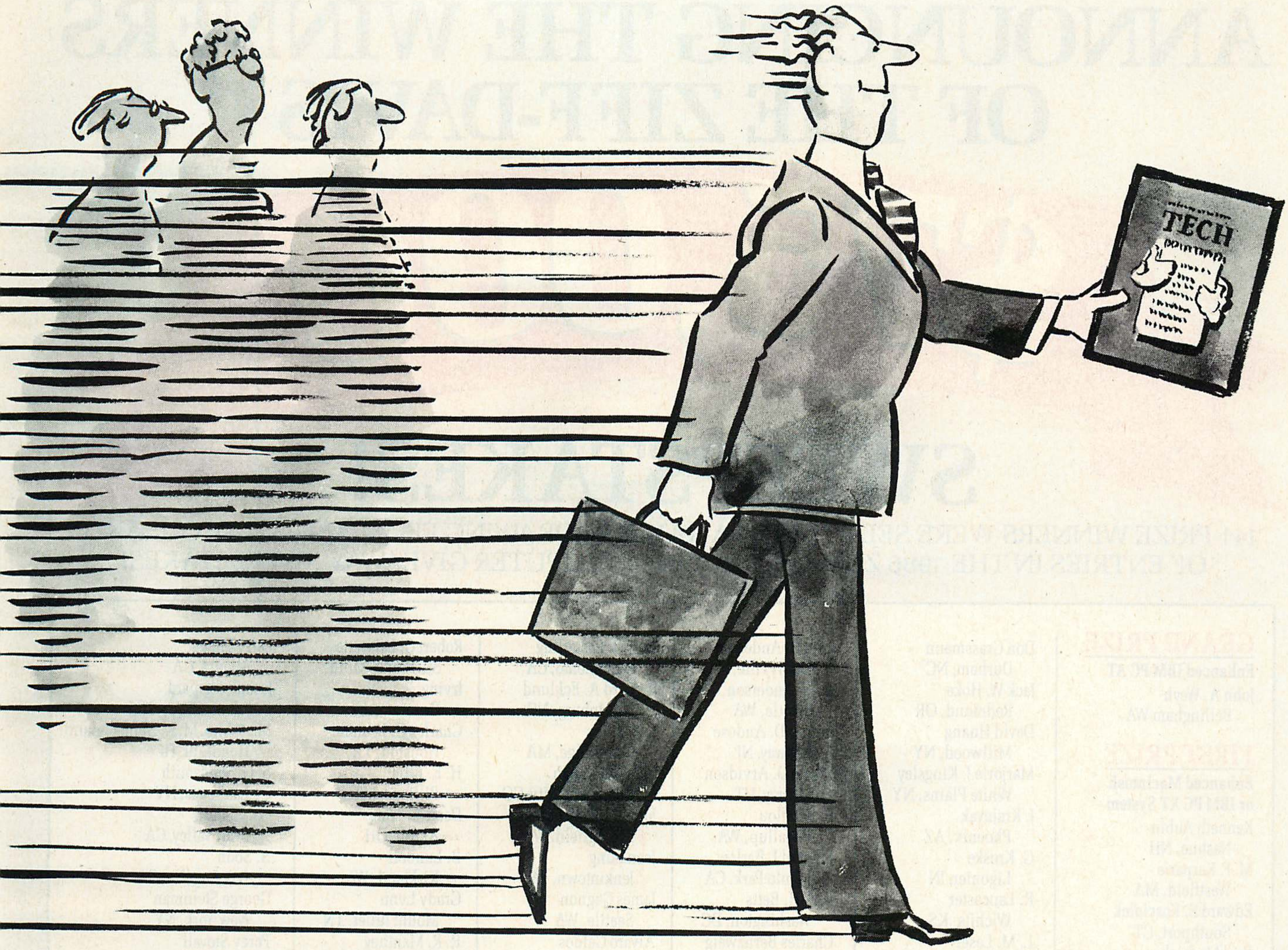

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CONGRATULATIONS!

Even arithmetic functions operate on lists. The addition operation takes a variable number of arguments and then returns their sum; for example, (+ 12 4 3) produces 19.

This uniformity in representing function calls and data values as lists produces an interesting effect. Given an expression such as

(CAR (CDR (A B C)))

how could LISP tell which portions of the list should be treated as function application and which as data? Are *CDR* and *A* function names or are they simple element values?

The LISP solution is simple; every atom and every list is evaluated unless otherwise specified. Numbers evaluate to themselves, and variables evaluate to their values. Every list, if evaluated, treats its first element as the function and applies it to the rest of the list.

To use the list itself as a constant argument, a special function is used to inhibit evaluation of the list. '(A B C) or, equivalently, (QUOTE (A B C)) expresses this quoting of the value. This evaluates to the list (A B C). The LIST function can construct a list of elements. Therefore, (LIST 'A '(C D)) produces the list (A (C D)).

FIGURE 1: *LISP Member Function*

```
(DEFUN MEMBER (A L)
   (COND ( (EQUAL L NIL)          ; this checks for an empty list
           NIL)                   ; NIL designates false
         ( (EQUAL A (CAR L))      ; A is the first element
           T)                     ; T designates true
         ( T                      ; always true, thus "otherwise "
           (MEMBER A (CDR L)))    ; make the recursive call on rest
   ))
```

The Member function in LISP is quite straightforward. It is usually implemented as a primitive function in most commercial LISP products.

Forcing evaluation of a list in LISP is the inverse action of quoting it. This can be expressed in one of two fashions. The LISP function EVAL used in the command (EVAL list) evaluates the list. The function APPLY applied to a list argument uses the first argument in the list as a function name and applies it to the remainder of the list. These functions are demonstrated below:

```
(EVAL '(CAR (A B C)))          -> A
(EVAL (LIST 'CAR '(A B C)))    -> A
(APPLY 'CAR '(A B C))          -> A
(EVAL '(1 2 3))                -> error
```

The ability to construct a data list then evaluate it is incredibly powerful. It allows a LISP program to construct another LISP program, and then execute it. It can be used for object-oriented programming by storing accessor functions in the data object.

To express a conditional case selection in LISP, the COND expression is used, as shown below:

```
(COND    ( <test 1> <result 1> )
         . . .
         ( <test n> <result n> )
)
```

The first <**test**> expression that is evaluated to true then causes the value of the <**result**> expression to be returned as the overall result.

Figure 1 shows how LISP would implement the **Member** function mentioned earlier. It actually is a primitive function in most LISP implementations.

The recursive function exactly follows the recursive list decomposition.

The DEFUN function in LISP is the common way to name and define a new function. An anonymous function value can be defined with the LAMBDA function. It is used to construct a function value that can take parameters and return a result when called. For example,

```
(LAMBDA (X) (+ 1 X))
```

defines a function that returns a number with a value one larger than that passed to it as an argument.

The preceding description of LISP is only a glimpse of a very broad language concept. The fundamental architecture of the language is very different from other languages. LISP encourages a radically different method of problem solving. Despite this difference, it has enough of the programming constructs to support many different programming styles, such as object-oriented programming, logic programming (as in Prolog), and even some classical FORTRAN-style programming.

LOGIC PROGRAMMING

Prolog is the result of collaboration between researchers from the University of Marseilles and the University of Edinburgh in the early 1970s. It encourages a much more stylized approach to problem solving than does LISP. In return for this, it provides a higher degree of programming support. (See "Programming in Logic," Michael Covington, December 1985, p. 82, and January 1986, p. 145.)

Prolog (whose name derives from *pro*gramming *log*ic) is based on logic. Writing programs in Prolog is similar to writing logical rules in a restricted mathematical logic. Running a Prolog program is akin to using the logical rules to prove certain conclusions.

Prolog programs consist of facts: "John is the father of Mary;" and rules: "if X is the father of Y and Y is the father of Z, then X is the grandfather of Z." A rule describes when certain conclusions can be drawn on the basis of available facts. X, Y, and Z are variables that behave as wild cards and could each match any person. In Prolog, this fatherhood knowledge would be written as follows:

```
father (john,mary).
grandfather (X,Z) :-    father (X,Y),
                        father(Y,Z).
```

The line **father (john,mary)** is a predicate asserting a relationship between **john** and **mary**. The term **father** has no significance beyond how we have defined it in our rules. The grandfather rule should be read as "Conclude that X is the grandfather of Z if X is the father of Y and Y is the father of Z." For any given group of people X and Y, the goal of concluding **grandfather (X,Z)** is met if the subgoals **father (X,Y)** and **father (Y,Z)** can be met.

To prove something, the goal has to match a fact in the database or match the goal of a rule where all its subgoals are themselves provable. When a question is posed, Prolog automatically searches the database of facts and rules with the goal of proving that the answer to the question is yes. This proof process is called *backward chaining*—working backward from the desired conclusion looking for rules or facts that will make it true.

To help illustrate the backward chaining process, consider the following father/child relationships:

```
father (john,mary).
father (fred,herbert).
father (john,fred).
grandfather (X,Z) :-  father (X,Y),
                      father (Y,Z).
```

In this simple case, the relationship **father (john,harvey)** is provable only if it explicitly occurs as a fact in the database. Prolog begins searching through the facts and rules one by one and returns no as the answer.

If the question **grandfather (john, herbert)** is posed, the goal **grandfather (X,Z)** applies, because the variables X and Z could match **john** and **herbert**. By the rule, **grandfather (john,herbert)** is the conclusion if a match can be found for the variable Y that proves **father (john,Y)** and **father (Y,herbert)**. Prolog searches the database and finds **father (john,fred)** and **father (fred,herbert)** and returns true.

Finding this solution did not occur immediately. In searching sequentially through the database trying to find a match for the variable Y, the program first came across the **father (john,mary)** fact. This led to a search that would prove **father (mary,herbert)**, because this would have completed the proof process. When this was unsuccessful, Prolog automatically backtracked, admitting defeat for that possible match and continuing the search for another solution to **father (john,Y)** as well as a solution to **father (Y,herbert)**.

Variables can be used in asking a question as well as in stating a rule. To find all of john's children, the following question could be posed: **father (john,**

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X). The variable X can match any second argument. Prolog will search sequentially through all facts and rule goals and report all matches for X. In this case, Prolog would return

X = **mary**
X = **fred**

Prolog's search for a proof is unrelenting. Every fact and rule in the database is tried. Every possible match for a variable is attempted.

This proof process, with powerful pattern matching to determine relevance and automatic backtracking to recover from failure, is Prolog's major contribution. It is a potent model for representing and applying knowledge.

As is the case in LISP, lists are an important data structuring concept in Prolog. A list in Prolog is a sequence of elements, such as

[tennis, baseball, golf].

The CAR and CDR functions of LISP have an analog in Prolog. Using variables X and Y in the pattern [X | Y], X matches the first element of the list, and Y matches the rest of the list. For the tennis, baseball, golf list, X would match **tennis** and Y would match the sublist **[baseball, golf]**.

The member function is easily stated in Prolog:

```
member (X, [ X | Y ]) .
member (X, [ Z | Y ]) :-     member (X, Y).
```

The first rule states that X is a member of the list if it occurs as the first element of the list. The second rule defines the recursive case; that is, X is a member of a list if it is a member of the rest of the list.

Consider the example of proving the property **member** (1, [2,1,3]) as a goal. Prolog would fail in its attempt to match the goal with the first fact—1 is not the first element of the list. It would, however, successfully match the goal of the second rule, with X = 1 and Z = 2 and Y = [1,3]. This match would generate the subgoal **member** (1, [1,3]). In this instance, the first fact applies, and the proof is completed.

By leaving any one argument as a variable, Prolog solves for the variable, determining all possible matches for the variable. Asking Prolog to prove **member**(X, [2,1,3]) produces a yes answer with three different matches for X: X = 1, X = 2, and X = 3. A request to prove **member** (1, [2, X, 3]) produces X = 1. An attempt to prove **member** (1,X) in order to find all of the lists in which the number 1 is a member would produce the correct answer, although Prolog would never complete the request. It would successively report matches for X of

X = [1 | X1]
X = [X2, 1 | X3]
X = [X4, X5, 1 | X6]

etc. These are the lists in which the number 1 would appear in the first position of an arbitrary list, then in the second, and so forth.

As is the case for LISP, a Prolog program can retrieve, manipulate, evaluate, and construct facts and rules. A program can dynamically alter the set of rules or facts or even change the evaluation strategy that Prolog uses in searching for applicable rules.

To a great extent, deduction from a set of rules in Prolog follows standard mathematical rules of deduction. Prolog provides a very high level of support for stating programs as rules—separating flow of control from essential aspects of the algorithms. Backward chaining deduction, pattern matching to determine relevance, and backtracking to search for solutions are all very common AI paradigms. Although all of these problem-solving approaches can be

programmed in LISP (and have been many times), Prolog elevates this deduction process to a conceptual model for programming. In doing so, it can provide a high degree of support.

Unlike in mathematical logic, however, the order in which rules are stated in Prolog can influence the outcome of a solution. In the worst case, incorrect order of rules may cause Prolog to loop infinitely. In almost all cases, the ordering has a major impact on how quickly Prolog finds solutions. Prolog's propensity for finding *all* solutions is frequently unnecessary and unwanted; often, any one solution is acceptable. To avoid the time-consuming process of continuing to search for solutions once one has been found, Prolog includes a **cut** function to cease further searching. As the programmer starts to worry about these practical concerns of rule order and cutting off searches early, some of the gains of logic programming are sacrificed.

UNLEARNING TRADITION

LISP and Prolog both allow programs and data to be manipulated in a uniform way. Learning either language involves unlearning many traditional programming techniques. Thinking recursively about data structures and program design takes some time to get used to. It can, however, result in a generous payoff in program compactness and clarity of program structure.

LISP and Prolog have very weak notions of data typing. This weakness lets the languages define very general list operations over lists of any type and to call functions with different argument types or different numbers of arguments. This is at the expense of the greater syntax checking skills of a more strongly typed compiler or interpreter. Errors not caught syntactically must be caught as runtime bugs.

AI programming techniques, such as recursively structuring programs and data, dynamic construction of objects, deduction, backtracking, and pattern matching can be used in a language such as C. The expression of such techniques is rather tedious and clumsy, but possible. Recursive list operations, for example, can be implemented in C using UNION data structures.

The higher degree of AI support in LISP and Prolog is traded for some aspects of inefficiency when compared with traditional programming languages. For LISP, dynamic construction of list values in an arbitrary way makes LISP memory hungry and requires time-consuming garbage collection at runtime. This garbage collection reclaims allocated lists to which the program no longer refers. Although storage management is quite efficient, using Prolog as a logic programming language can lead to time-consuming and unnecessary backtracking for solutions.

For PC-based AI products, efficiency in memory consumption and performance is an important issue. As PCs continue to have better performance and larger memory addressability, this will be less of a problem. For now, however, it limits the size of applications that can be written and run effectively using LISP or Prolog on PCs.

One solution to this dilemma is to develop AI programs in LISP or Prolog, then, after development is complete, reengineer and recode the design for C or Pascal. This would take advantage of the flexibility of concepts and data structuring of the AI languages during the turbulent design phase, and then would opt for the runtime efficiency of C or Pascal.

Richard Schwartz, Ph.D., and Robert Shostak, Ph.D., are vice presidents of software development and cofounders of Ansa Software.

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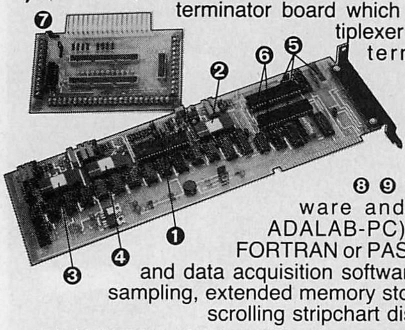

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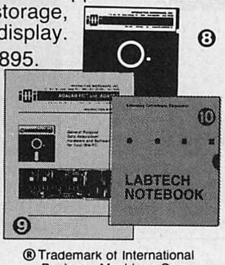

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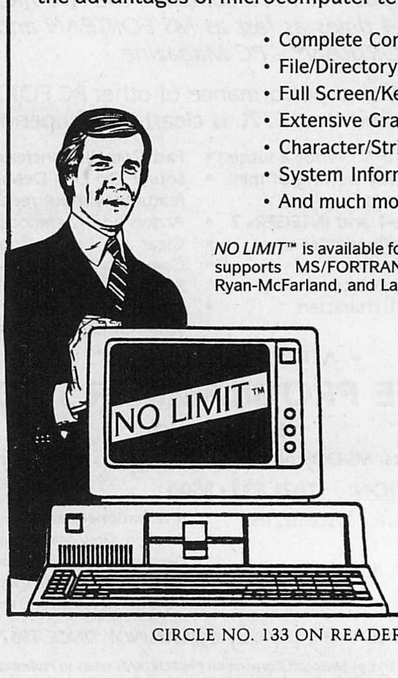

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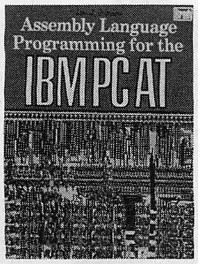
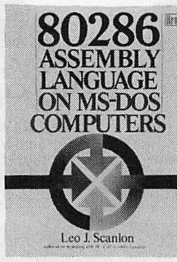
Some Assembly Required

The 80286 is the topic of three recent books: two, by popular author Leo Scanlon, do not go quite far enough; the third, by two Intel engineers, is an excellent, candid account of the 80286.





Assembly Language Programming for the IBM PC AT
Leo J. Scanlon (Brady Communications Company, Inc., 1986), 442 pages; paper, $21.95

80286 Assembly Language on MS-DOS Computers
Leo J. Scanlon (Brady Communications Company, Inc., 1986), 316 pages; paper, $21.95

The most noticeable feature distinguishing the iAPX 80286 from its older siblings is speed; it runs DOS software two to three times faster than the 8086/88. Because a more sophisticated DOS-compatible operating system does not yet exist, the most important distinguishing characteristic—the processor's ability to run in either real address mode or protected virtual address mode—has remained largely unused.

In real mode, the 80286 behaves as if it were simply a fast 8086/88. Its real mode instruction set is, with minor exceptions, a superset of the 8086's. Most well-behaved code written for the older devices will run unmodified on an 80286-based machine.

The protected mode marks a radical departure from previous architectures. Offering virtual memory, multitasking, and a sophisticated protection mechanism, it enables systems programmers to produce much more powerful operating systems.

An unsuspecting reader may assume from the titles that these books cover the full capabilities of the 80286 and reveal the secrets of its protected virtual address mode. This is not true, and it is unfortunate considering the author's background.

Leo Scanlon is a prolific author of assembly language texts for 8086/88 computers. Among his previous efforts are *IBM PC and XT Assembly Language* and *8086/88 Assembly Language Programming*, both of which have been well received. His two latest books, however, are little more than rewrites of the earlier works.

The author seems to contradict himself when he writes, "the protected mode is best left to designers of operating systems. Casual programmers should stay away from it. With this in mind, we will generally concentrate on the real address mode." Assembly language programmers are seldom "casual." The books suffer from this underestimation of their intended audience.

The books offer much, in spite of this limitation. The author's prose is easy to follow and noticeably devoid of jargon. Well-documented programming examples abound; most are useful utility routines. The AT book offers an optional $30 diskette containing source code and object code for the examples that are complete procedures.

Abundant tables help in using the books as a reference. A quick reference index of mnemonics and pseudo-ops appears on the inside back cover.

These two books are nearly identical through the first six chapters. Among the topics covered are: computer numbering systems, basic 80286 architecture, the macro assembler, the instruction set, high-precision mathematics, and data structures. The AT book then includes a good discussion of BIOS and PC-DOS interrupts; the MS-DOS book contains only the DOS interrupt discussion. The AT book continues with chapters on video, keyboard, and speaker operations. Both then discuss macros, object libraries, and the 80287 numeric coprocessor.

The instruction set chapter in the AT book is particularly well organized. Mnemonics are presented in functional groups rather than in alphabetical order. This pedagogical approach is far better than the usual reference manual ordering. As necessary, the reader can rapidly locate an instruction using the quick-reference index. The high-precision mathematics chapter also stands out. It includes routines for signed and unsigned 32-bit by 32-bit multiplication, 32-bit by 16-bit division, and 32-bit square root calculation.

The AT book contains more than 30 macros that are suitable for inclusion in a library. The source code for each is listed, along with a short reference description. The AT book's optional diskette contains the source code for this macro library. This book's chapter on video deals only with text-mode character graphics in the monochrome and color/graphics adapters.

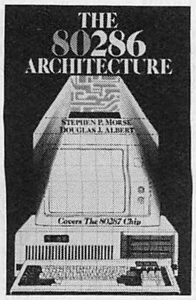
Sample problems are offered in the early chapters, and all of them are answered in an appendix. Regrettably, the number of exercises offered is limited and tends to be easy. Programming, particularly assembly language programming, is learned by writing and debugging code. Exercises of varying degrees of difficulty should be available, along with their solutions.

The two books differ in that they are written for separate macro assemblers. The AT book uses version 2.0 of the IBM Macro Assembler; the MS-DOS book uses version 3.0 of the Microsoft Macro Assembler. Each book contains a chapter specific to the particular assembler supported. The MS-DOS book devotes a short chapter to a discussion and comparison of batch files and the Microsoft program maintenance utility MAKE. The AT book treats structured programming based on IBM's Structured Assembly Language Utility (SALUT). The two books would have been as strong without these chapters.

Both books are recommended in view of their fine treatment of the real address mode—the reader simply must be willing to do without a discussion of the protected virtual address mode. Their organization makes them good reference works, and they complement the volume every 80286 programmer should have: *iAPX 286 Programmer's Reference Manual* (Intel, 1985).

The 80286 Architecture

Stephen P. Morse and Douglas J. Albert (Wiley Press, 1986), 279 pages; paper, $24.95



This book by Stephen Morse, principal architect of the Intel 8086, and Douglas Albert, former staff engineer at Intel, is a gem. The authors share their experience and candid insights including design trade-offs and flaws of the iAPX 80286. The book is not a programming manual—few programming examples are included and no sample exercises are given. The authors spend as much effort describing *why* a particular instruction exists or works in a certain way, as they do about *how* it works.

The first four chapters cover the operation of the 80286 and 80287 in real address mode. The authors compare and contrast the 80286 and 80287 with their older relatives—with whom a reader is likely to be familiar—the 8086/88 and 8087. These early chapters detail 80286 and 80287 architecture by thoroughly exploring their addressing modes and basic instruction sets.

Instructions are discussed in functional groups. Examples clarify each instruction. The treatment of synchronization on a multiprocessor system, although short, is nicely done. The 80286-unique, high-level language support instructions (BOUND, ENTER, and LEAVE) also are thoroughly covered.

Memory management, protection, and multitasking are presented clearly and with a level of detail comparable to that found in reference manuals. A reader with a systems programming background will profit greatly from this chapter. One warning: this is not speed-reading material. Be prepared to make several slow passes.

In the "Building a Computer" chapter, Morse and Albert describe how the 80286 and 80287 devices interface with support components to make a complete microcomputer system. The discussion includes the 80286 bus, ROM and dynamic RAM, I/O devices and interrupts, and direct memory access.

The book concludes with six rather lengthy appendixes. The first two contain the Intel reference manual's instruction set tables. Two others describe the structure of 80286 and 80287 opcodes. Another describes intertask message passing and includes pseudo-code and 80286 assembly language code for a simple implementation. The last appendix is a fine glossary. Finally, its exhaustive 15-page index makes this excellent reference work complete.

The 80286 Architecture is highly recommended. Every 80286 and 80287 assembly language programmer should have a copy. Its style, readability, generous use of quality figures and tables, and excellent index make this book an important addition to the library of any 80286 owner.

—JEFFERY W. WILSON

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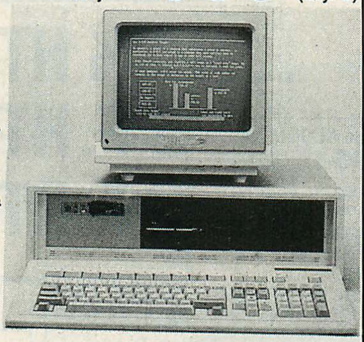

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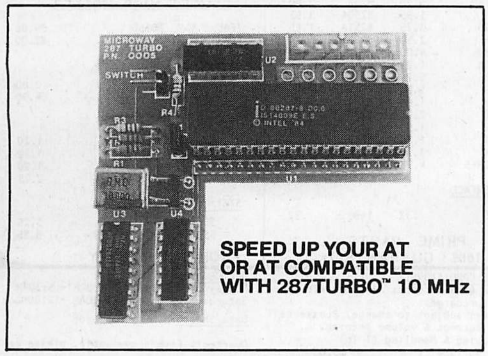

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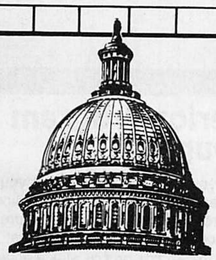

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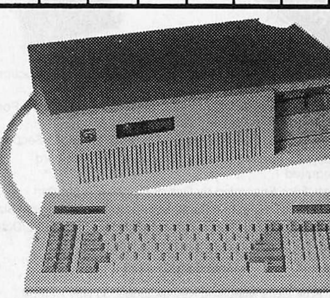

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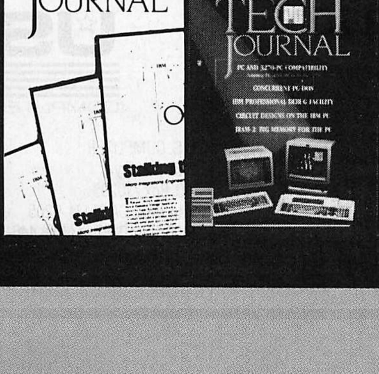

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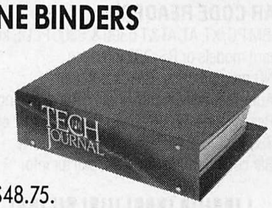

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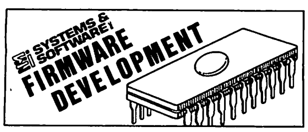

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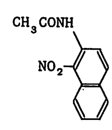

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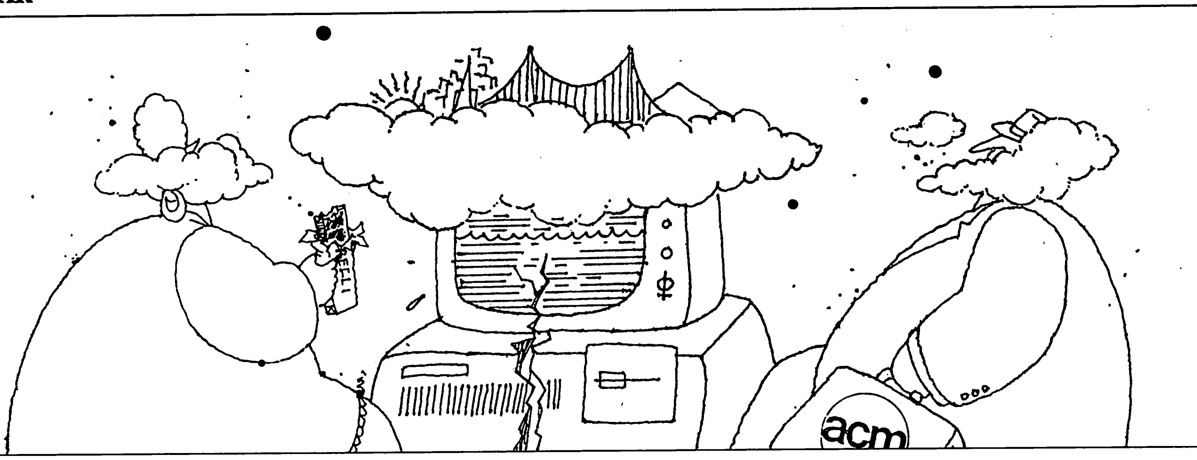

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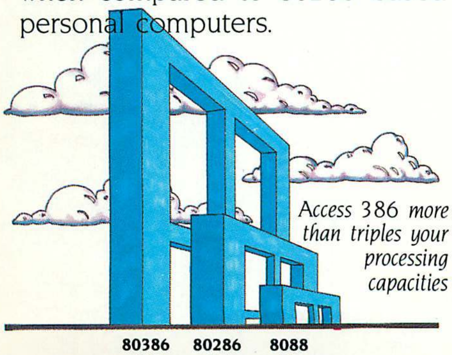

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